

High-efficient single-phase, non-isolated, multi-input microinverter with common ground for photovoltaic systems

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ABSTRACT

Single-phase non-isolated microinverters used in photovoltaic (PV) systems commonly encounter two persistent challenges: High-frequency leakage current and fluctuating power delivery. This paper presents a novel single-phase, non-isolated multi-input microinverter topology with a common-ground structure that effectively eliminates ground leakage current without requiring additional active components. The proposed microinverter architecture integrates a dual-boost configuration and uses only four active switches. This is especially advantageous in terms of the component count, which is beneficial to enhance reliability, reduce cost, and simplify the overall system design. With one, two, or four PV inputs, it can operate without interruption under unbalanced voltage or partial shading and even if some inputs drop to zero. A tailored modulation scheme minimizes conduction losses while maintaining a stable direct-current (DC)-link voltage, and a decoupling capacitor efficiently absorbs the single-phase pulsating power, thus overcoming one major limitation in existing microinverter designs. By validating with a 1-kW GaN-based prototype, both the simulated and experimental results demonstrate its high efficiency, robustness, and practical suitability for cost-effective PV applications, with a peak efficiency value of 94.8%.

1. Introduction

Photovoltaic (PV) modules integrated with microinverters are reliable solutions for distributed renewable generation [1]. Inverters, as the core components of such systems, are generally classified as central inverters [2], string inverters [3], and microinverters [4]. Among them, microinverters are preferred in residential PV modules due to their modularity, independent maximum power point tracking (MPPT), and flexibility. Since compactness and high efficiency are critical, single-stage microinverters are advantageous over two-stage designs as they have less components and conversion stages [5], especially for those with non-isolated configurations which could further improve the efficiency and compactness [6]. Nowadays, single-stage, non-isolated microinverters are being a growing focus [7].

As all we know, one major challenge in transformerless topologies is the leakage current. In full-bridge inverters, mitigation relies on switching strategies [8] or improved topologies [9], such as the H5-type with 5 switches, H6-type with 6 switches, and highly efficient and reliable inverter concept (HERIC) inverters. Although they are capable of overcoming this limitation, voltage boosting is

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lacking. Tian et al. [10] demonstrated that the leakage could be effectively suppressed by creating a common ground between PV and grid leakage, which has driven increasing interest in dual-grounded topologies. Even though half-bridge inverters with grounded direct-current (DC) midpoints have been proven to mitigate leakage [11], they incur higher losses and require bulky filters. Thus, unipolar H-bridges remain favorable once the leakage can be suppressed. One viable way is using auxiliary switches to isolate PV modules during null states [12]. However, it leads to increased switches and complexity. Designs such as Z-source [13], split-source [14], and their derivatives [15] are capable of reducing switches but also face issues like leakage, input current reversal, or increased complexity. Other solutions include three-switch [16], four-switch [17], and five-switch [18] inverters, each with trade-offs in gain, ripple, or stress. Virtual-ground-based designs [19] and the single-phase neutral-point-clamped (NPC) inverters [20] mitigate the leakage but demand voltage balancing and lack boosting. Flyback-based inverters [21] provide higher gain but have more complex designs. Moreover, multi-input microinverters able to integrate multiple PV sources are becoming more and more attractive in recent years. But they still encounter similar limitations. For example, dual-input microinverters [22] suffer from high switch counts, while three-level [23], cascaded GaN-based [24], and bidirectional [25] inverters exhibit increased complexity or limited PV suitability; some flyback converters adopt time-sharing control but require additional buffering components. Therefore, a more robust solution is such a topology that can simultaneously process multiple PV inputs, tolerate shading or mismatch, and deliver boosted alternating-current (AC) outputs with low leakage and minimal switches.

To fill this gap, a single-phase, non-isolated, multi-input microinverter with common ground is proposed in this paper, which can simultaneously realize voltage boosting and leakage current elimination with only four active switches. It is demonstrated that such microinverter can effectively suppress the high-frequency leakage while no auxiliary devices are required. With flexible multi-input operation, it can sustain power delivery even when one input is shaded or disconnected. The experimental results show that the proposed microinverter performs superior to the existing ones, with smaller components, higher gain, improved leakage suppression, and enhanced efficiency.

2. Operation, control, and performance characterization of the proposed microinverter

Fig. 1 illustrates the proposed high-efficient non-isolated, multi-input microinverter featuring an active power decoupling mechanism. The topology exhibits a vertically symmetrical structure comprising four active power switches (S_1 – S_4) and two diodes (D_1 and D_2), which serve to block the reverse current flow to the DC input sources. The inclusion of parasitic capacitances (C_{PV1} and C_{PV2}) across the PV inputs ensures voltage stabilization and facilitates smooth power delivery, particularly under partial shading conditions. The AC output is connected to a low-pass inductor-capacitor (LC) filter, which effectively attenuates high-frequency switching harmonics and improves the quality of the output current waveform delivered to the grid.

2.1. Operation analysis

The proposed microinverter circuit operates in dual-boost (DB) mode, where four independent DC sources are utilized. Four distinct switching states are generated by appropriately controlling the H-bridge. These states are denoted as active-2 (10), null-1 (00), active-1 (01), and null-2 (11). The binary indices in braces represent the gate signals applied to switches S_1 and S_3 , respectively, while $S_2 = S_1$ and $S_4 = S_3$ operate as their complements. Here, the superscript bar ($-$) denotes the logical complement or inverse of the corresponding switching signal, meaning that each switch pair in the same inverter leg operates in a complementary manner to prevent simultaneous conduction and DC-link short-circuiting. Each state corresponds to a unique circuit configuration, as illustrated in Fig. 2. The selection of the state in each switching period is determined by the control strategy.

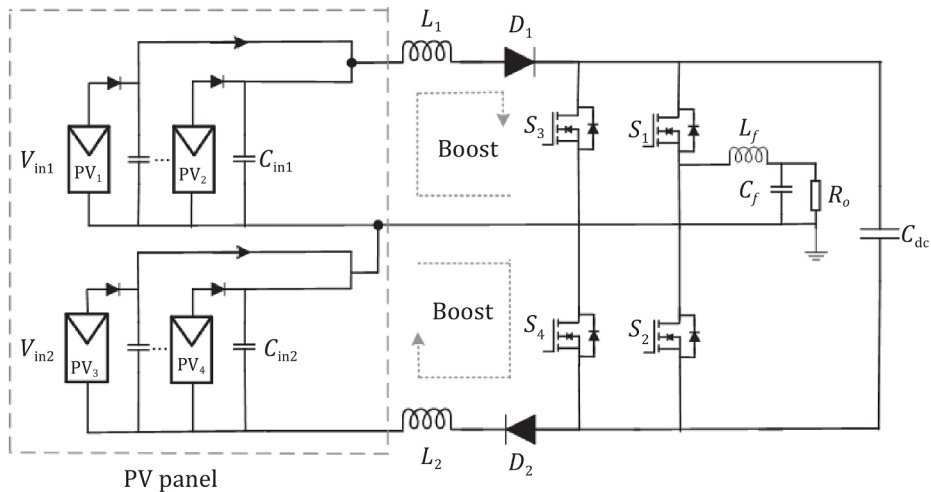


Fig. 1. Diagram of the proposed non-isolated, multiple-input microinverter.

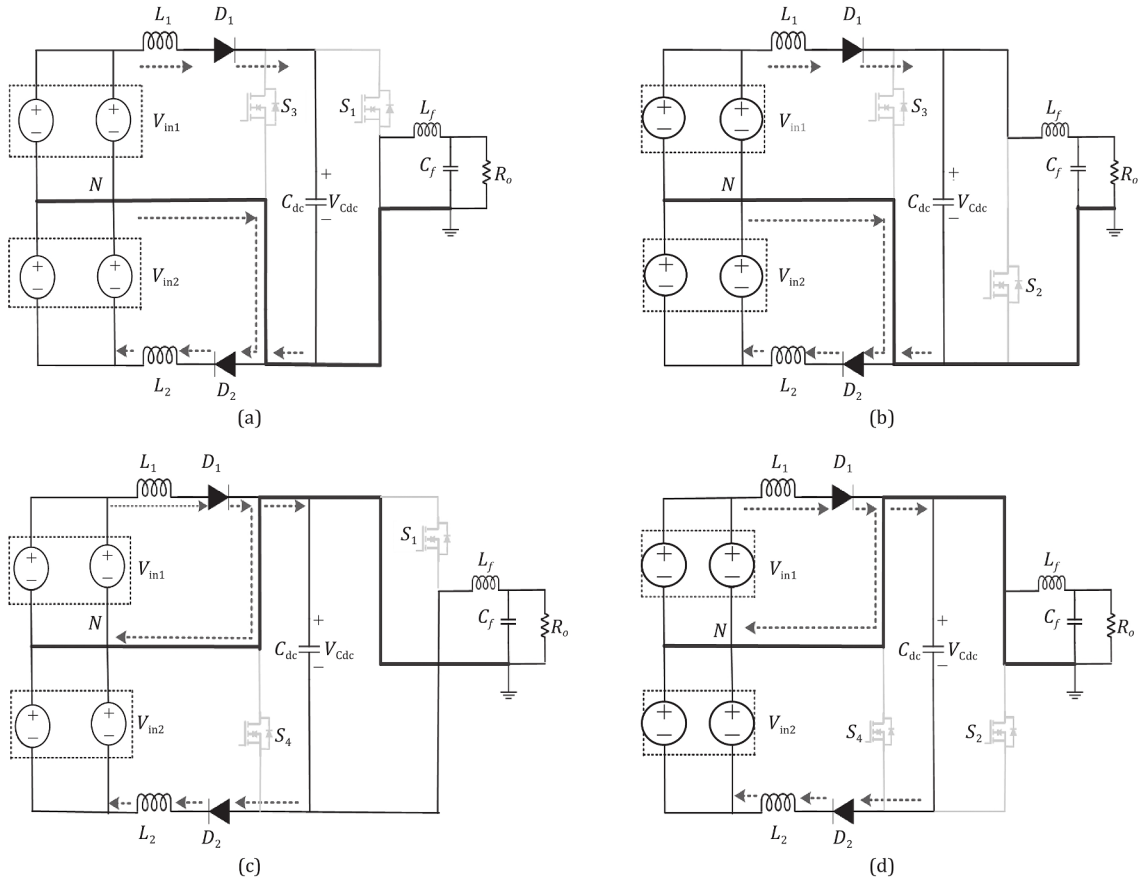


Fig. 2. Switching states of the lower and upper circuits of the proposed microinverter: (a) null-1 (00), (b) active-1 (01), (c) active-2 (10), and (d) null-2 (11).

Transformerless single-phase PV inverters have been widely used due to their high efficiency and low costs [26]. However, they suffer from common-mode (CM) leakage currents, which raise safety concerns. A kind of low leakage current active NPC circuits in transformer-less single-phase inverters has been proposed in Ref. [27]. Doubly grounded topologies, where both the PV array and the inverter output are connected to the ground, have been demonstrated to be an effective solution to eliminate such CM leakage and thus enhance safety. Based on this, in our proposed microinverter, a pulse-width modulation (PWM) scheme is combined with time-sharing MPPT to regulate the H-bridge. The switching logic follows distinct sequences depending on the polarity of the output current's fundamental cycle. During the positive fundamental half-cycle (FHC), the switching states change through (00, 10, 11), while in the negative FHC, they follow the sequence (00, 01, 11). Its operation in the positive FHC can refer to Figs. 2(a) and (b). During these states, the input voltage V_{in2} charges the inductor L_2 through the switch S_4 , while L_1 discharges (off-state) either into the DC-link capacitor C_{dc} (in the null state) or into the filter capacitor C_f (in the active state). Later, in Fig. 2(d) (corresponding to the null-2 state), V_{in1} charges (on-state) L_1 via S_3 , and L_2 discharges into C_{dc} . Similar operation conditions occur during the negative FHC, with the switching roles of L_1 and L_2 reversed. These operational details are summarized in Table 1 based on the states and FHC.

To characterize the switching dynamics, several key parameters are defined as follows: The average inductor currents during the positive and negative FHCs are denoted as I_{Lx}^+ and I_{Lx}^- , respectively, where $x = 1, 2$; I_c indicates the average current through the DC-link capacitor; I_o and V_o represents the output current and voltage of the microinverter, respectively. By applying the volt-second balance principle to both inductors over a switching period T_s , the following expressions are obtained:

$$V_{in1}d_3T_s + (V_{in1} - V_{Cdc})d_{L1}T_s = 0 \quad (1)$$

$$V_{in2}d_4T_s + (V_{in2} - V_{Cdc})d_{L2}T_s = 0 \quad (2)$$

where V_{Cdc} represents the DC-link voltage; d_3 and d_4 are the duty ratios (fractions of T_s) for the conduction of switches S_3 and S_4 , respectively, d_{L1} and d_{L2} are the respective discharging duty ratios of L_1 and L_2 , and their corresponding time intervals are denoted as d_3T_s , d_4T_s , $d_{L1}T_s$, and $d_{L2}T_s$, respectively. As shown in Fig. 2, we have $d_{L1} \leq 1 - d_3$ and $d_{L2} \leq 1 - d_4$. These relationships depend on whether the inductors operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), with equality in CCM and strict inequality in DCM. During the positive FHC, d_3 indicates the duration of the null-2 state, while d_4 covers the combined

Table 1
Charging and discharging states of all the components.

Component/parameter	Positive FHC ($V_o > 0$)			Negative FHC ($V_o < 0$)		
	Null-1 (00)	Active-2 (10)	Null-2 (11)	Null-1 (00)	Active-1 (01)	Null-2 (11)
L_1	Non-active	Non-active	Active	Non-active	Active	Active
L_2	Active	Active	Non-active	Active	Non-active	Non-active
C_{dc}	Active	Non-active	Active	Active	Non-active	Active
I_c	$I_{L_1}^+$	$I_o - I_{L_1}^+$	$I_{L_2}^+$	$I_{L_1}^-$	$I_o - I_{L_2}^-$	$I_{L_2}^-$
Duration	$M_{dc1}T_s$	$(d_1 - M_{dc1})T_s$	$(1 - d_1)T_s$	d_1T_s	$(M_{dc2} - d_1)T_s$	$(1 - M_{dc1})T_s$

intervals of the null-1 and active-1 states. Under sinusoidal pulse-width modulation (SPWM), they typically satisfy $d_3(t) < 0.5$ with $d_4(t) = 1 - d_3(t) > 0.5$, indicating that the inductor L_2 is responsible for boosting the DC-link voltage. Consequently, V_{Cdc} exceeds twice the PV input voltage: $V_{Cdc} > 2V_{in}$ (V_{in} indicates either V_{in1} or V_{in2}). However, similar to conventional SPWM-based inverters, the resulted DC-link voltage varies with the time. To maintain stable operation, V_{Cdc} must remain larger than both $2V_{in1}$ and $2V_{in2}$. Under these conditions, L_1 operates in DCM since its discharging duty ratio d_{L_1} remains less than $d_3(t)$, and their combined value stays below unity. In contrast, L_2 may operate in either CCM or DCM depending on its average current level and instantaneous current ripple. The current ripple for the inductor L_2 during the switching cycle is given by

$$\Delta I_{L_2}(t) = \frac{V_{in2}T_s}{2L_2}d_4(t) \quad (3)$$

At the zero-crossings of the output voltage V_o , the ripple current may exceed the average current I_{L_2} , causing the inductor L_2 to enter DCM. During the negative FHC, the situation is reversed: L_2 remains in DCM, while L_1 may alternate between DCM and CCM, depending on the ripple profile of its current. Although simultaneous DCM operation of both inductors is possible, such a situation typically results in higher conduction losses. To minimize these losses and suppress DC-link voltage fluctuations, a modified pulse-width modulation (MPWM) strategy is applied. MPWM ensures that the DC-link voltage V_{Cdc} remains well regulated over both positive and negative FHCs, contributing to improved efficiency, reduced losses, and enhanced system reliability.

M_{dc1} (DC offset/bias applied during the positive FHC in MPWM) and M_{ac} (modulation index) are essential in regulating inductor current balance and preventing DCM operation. During the positive FHC, the average current in L_2 , i.e. $I_{L_2}^+$, is typically higher than that in L_1 , i.e. $I_{L_1}^+$, increasing the risk of L_2 entering DCM. This risk can be mitigated by increasing M_{dc1} and M_{ac} to raise the energy in L_1 , i.e. $I_{L_1}^+$, and avoid DCM operation of L_2 . To ensure balanced operation and minimize DCM of L_2 , the selected inductance values for L_1 and L_2 should satisfy the following condition:

$$L_1 = L_2 \geq \frac{(\rho + 1)T_s M_{dc1}^2 V_{in}^2}{2P_o(1 - M_{dc1})} \quad (4)$$

where ρ is a design ratio for average inductor currents, P_o is the average output power of the microinverter, and $V_{in} = V_{in1} = V_{in2}$ is the average input voltage assumed to simplify the mathematical expressions.

Based on the modulation strategy described above, M_{dc1} primarily influences the DC-link offset and current balance between L_1 and L_2 , while M_{ac} governs the output voltage amplitude. Considering these modulation effects, (5) can be derived and further simplified as (6).

$$V_{in2}(1 - M_{dc1})T_s + (V_{in2} - V_{Cdc})M_{dc1}T_s = 0 \quad (5)$$

$$V_{Cdc} = \frac{V_{in2}}{M_{dc1}} \quad (6)$$

Similarly, in the negative FHC, the average current $I_{L_1}^-$ is usually larger than $I_{L_2}^-$. Therefore, L_2 needs to be boosted to prevent L_1 from operating in DCM. This means that ensuring L_1 consistently operate in CCM yields

$$V_{Cdc} = \frac{V_{in1}}{1 - M_{dc2}} \quad (7)$$

where M_{dc2} is the DC offset/bias applied during the negative FHC in MPWM. It is realizable to regulate the DC-link voltage V_{Cdc} independently of input voltages V_{in1} and V_{in2} by adjusting M_{dc1} and M_{dc2} in MPWM. These indices act as CM signals and do not affect the differential output, thus allowing the AC voltage to remain stable. This modulation flexibility enables reliable operation even under fluctuating input conditions by setting V_{Cdc} via (6) in the positive FHC and (7) in the negative FHC. Elaborately-designed system parameters are required to guarantee that V_{Cdc} has a low-frequency ripple below 1%. When multiple PV sources are connected, this voltage regulation contributes to improved energy efficiency and steady-state performance. In contrast, for a single PV source, it is unnecessary to perform such independent tuning of M_{dc1} and M_{dc2} . However, a sufficiently large DC-link capacitor C_{dc} is required to absorb the second-order ripple and suppress midpoint voltage variations at the node N . The proper selection of C_{dc} is critical to ensure stable operation and efficient power delivery.

Accordingly, the required minimum capacitance can be obtained as

$$C_{dc,min} \geq \frac{25}{f_1} \left| \frac{(1 - M_{dc2})^4 T_s}{M_{dc2} L_2} - \frac{4M_{ac}}{\pi R_o} \right| \quad (8)$$

where f_1 is the line/fundamental frequency and equal to 50 Hz or 60 Hz in this paper. Equation (8) indicates the sizing condition derived from modulation indices and ripple suppression. Then, the DC-link capacitor can also be sized from the power and allowable voltage ripple constraint and expressed as

$$C_{dc} \geq \frac{P_o}{2\pi f_1 V_{Cdc} \Delta V} \quad (9)$$

where ΔV denotes the permitted peak-to-peak second-order ripple.

To estimate the current stress on the magnetic components under rated operation, the peak and average values of the inductor current were theoretically calculated, which is also beneficial to determine the initial sizes of the inductors and ensure operation within the linear region of the core materials. The calculation details are as follows. The duty ratio d_{L_1} of the auxiliary switch is first calculated as (10) shows. Correspondingly, the peak current I_{L_1-pk} and average current $I_{L_1}^+$ in the inductor L_1 are given by (11) and (12), respectively. Assuming the total power is balanced across both inductors, the required total current satisfies (13). Therefore, the average current $I_{L_2}^+$ through L_2 can be calculated as (14).

$$d_{L_1} = \frac{V_{in1} M_{dc1}}{(V_{Cdc} - V_{in})} \quad (10)$$

$$I_{L_1-pk} = \frac{V_{in1}}{L_1} M_{dc1} T_s \quad (11)$$

$$I_{L_1}^+ = \frac{1}{2} I_{L_1-pk} (M_{dc1} + d_{L_1}) \quad (12)$$

$$I_{L_1}^+ + I_{L_2}^+ = \frac{P_o}{V_{in}} \quad (13)$$

$$I_{L_2}^+ = \frac{P_o}{V_{in}} - \frac{V_{in} T_s M_{dc1}^2}{2L_1(1 - M_{dc1})} \quad (14)$$

Based on (10)–(14), the inductor values, which can ensure that the current ripple and saturation levels are always acceptable during rated operation, are determined.

2.2. Control strategy

To ensure smooth and stable operation, four switching devices (S_1 – S_4) and multiple passive components have been included in the proposed microinverter. The inductors (L_1 and L_2) perform the DB function to regulate the DC-link voltage, while the parasitic input capacitances (C_{PV1} and C_{PV2}) represent the natural coupling between each PV module and the ground. Their inclusion ensures accurate modeling of the leakage current behavior. The DC-link capacitor (C_{dc}) stabilizes the boosted DC voltage, and the resistor-capacitor (RC) output filter attenuates switching harmonics in the AC output. These elements work together to support the control strategy for sinusoidal reference signal generation and voltage regulation. The overall control strategy of the proposed microinverter is illustrated in Fig. 3. It is designed not only to generate the sinusoidal reference signal and perform AC voltage regulation and power conversion with

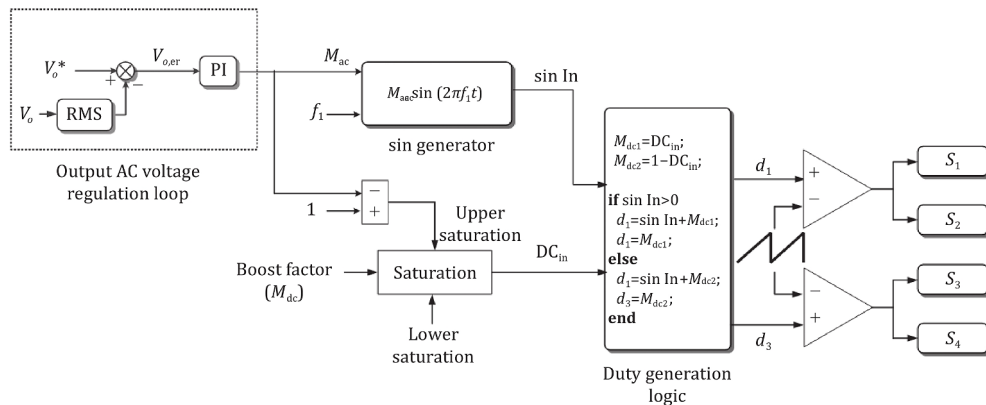


Fig. 3. Block diagram of the proposed microinverter control strategy.

duty cycle modulation, but also to form a feedback control loop.

The generated sinusoidal reference signal for the PWM controller is formulated as

$$\sin \text{In}(t) = M_{ac} \sin(2\pi f_1 t) \quad (15)$$

where the sinusoidal signal $\sin \text{In}(t)$ serves as the reference waveform for PWM generation. This signal governs the formation of modulation references $d_1(t)$ and $d_3(t)$, which are compared with a triangular carrier to produce the PWM switching signals for the microinverter. In the MPWM scheme, $d_1(t)$ is derived by adding a smaller DC offset M_{dc1} to the positive FHC and a larger offset M_{dc2} to the negative FHC of the reference waveform. Similarly, $d_3(t)$ incorporates the same offsets during opposite half-cycles to control the complementary leg. This approach enables balanced voltage boosting and minimizes common-mode voltage fluctuations in the microinverter output. The output voltage magnitude is directly related to both the modulation amplitude M_{ac} and the intermediate DC-link voltage V_{Cdc} , as follows:

$$d_1(t) = \begin{cases} M_{ac} \sin(2\pi f_1 t) + M_{dc1}, & 0 < t < \frac{1}{2f_1} \\ M_{ac} \sin(2\pi f_1 t) + M_{dc2}, & \frac{1}{2f_1} < t < \frac{1}{f_1} \end{cases} \quad (16)$$

$$d_3(t) = \begin{cases} M_{dc1}, & 0 < t < \frac{1}{2f_1} \\ M_{dc2}, & \frac{1}{2f_1} < t < \frac{1}{f_1} \end{cases} \quad (17)$$

$$V_o(t) = V_{Cdc}(d_1(t) - d_3(t)) \quad (18)$$

The DC modulation levels are defined as $M_{dc1} = \text{DC}_{in}$ and $M_{dc2} = 1 - \text{DC}_{in}$. Here DC_{in} is the modulation biasing (boost factor) introduced in the duty cycle logic of the MPWM scheme to ensure that the duty ratios remain within a valid bound of [0, 1]. The actual duty cycles are then determined based on the polarity of the sinusoidal reference signal, as follows:

$$\begin{cases} d_1(t) = \sin \text{In}(t) + M_{dc1} \\ d_3(t) = M_{dc1} \end{cases}, \text{ if } \sin \text{In}(t) > 0 \quad (19)$$

$$\begin{cases} d_1(t) = \sin \text{In}(t) + M_{dc2} \\ d_3(t) = M_{dc2} \end{cases}, \text{ else} \quad (20)$$

All these values have influence on the switching logic for the H-bridge. The control variable DC_{in} regulates the intermediate DC-link voltage V_{Cdc} by adjusting the boost level. An increase in DC_{in} leads to a higher V_{Cdc} , thus enhancing the output AC voltage. To maintain a regulated output voltage, a proportional-integral (PI) controller is implemented. It dynamically adjusts the modulation index M_{ac} by minimizing the error ($V_{o,er}$) between the actual output voltage V_o and the reference voltage V_o^* .

$$V_{o,er} = V_o^* - V_o \quad (21)$$

$$M_{ac} = K_p V_{o,er} + K_i \int V_{o,er} dt \quad (22)$$

where K_p is the proportional gain and K_i is the integral gain. The modulation index is bounded within $0 \leq M_{ac} \leq 1$ to prevent over-modulation and ensure safe operation. A boost factor M_{dc} , i.e., the DC modulation level M_{dc1} or M_{dc2} defined earlier, is also incorporated to improve the efficiency of power delivery by ensuring that the required DC-link voltage is achieved. The PWM signals generated by the control system as Fig. 3 shows are applied to the switching devices S_1 – S_4 to achieve regulated DC-AC power conversion. As shown in Fig. 1, at the output stage, an LC filter composed of C_f and L_f is used to attenuate high-frequency harmonics, while the inductors (L_1 and L_2) and input capacitors (C_1 and C_2) are adopted to boost and stabilize the voltage. A resistive element R_o is connected at the output to act as the load.

Fig. 4 illustrates the Bode analysis results of the proposed control system, showing both the magnitude and phase responses for the plant G_d , the PI controller C_z , the closed-loop transfer function G_{cl} , and the open-loop gain G_{ol} . As shown in Fig. 4(a), the system achieves a crossover frequency $f_c = 2.99$ Hz, indicating the bandwidth of the closed-loop system. It is also obvious that the gain margin (GM) is approximately 6.9 dB and the phase margin (PM) is around 95.4° . These results confirm that the designed control strategy provides a robust and stable response under expected operation conditions. Although sharp roll-off and resonance peaks are observed in the magnitude response at higher frequencies, they are mainly originated from the system dynamics and controller behavior and can be sufficiently attenuated to prevent instability. In the proposed strategy, such attenuation is partly originated from the natural damping introduced by the resistive load in the LC filter. Moreover, a low crossover frequency of 3.09 Hz is maintained, which lies far below the LC resonance frequency. This means that the resonance in the control loop can be effectively suppressed. In addition, the large PM (95.4°) and GM (6.7 dB) further guarantee that the high-frequency peaks remain harmless. This Bode analysis also validates the effectiveness of the PI controller in achieving desired dynamic performance and maintaining system stability. The resonance peaks

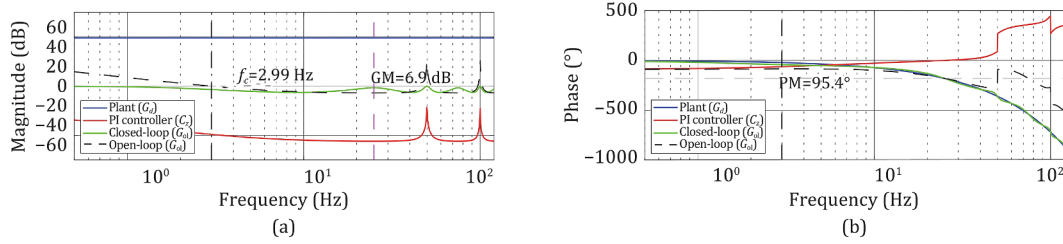


Fig. 4. Bode plots of the open-loop and closed-loop systems: (a) magnitude response and (b) phase response.

observed in the Bode response can be directly explained by the microinverter output stage dynamics, whose transfer function is given in (23). This model, representing a second-order LC filter followed by a resistive load, captures both the resonance characteristics of the filter and the natural damping due to the load resistance, thereby providing the theoretical basis for the peaks in the frequency domain.

$$G(s) = \frac{K}{L_f C_f s^2 + s \left(\frac{L_f}{R_o} + R_o C_f \right) + 1} \quad (23)$$

where K is the system gain factor derived from the DC-link voltage V_{Cdc} and given by $K = V_{Cdc}/\sqrt{2}$; s is the Laplace operator.

2.3. Performance characterization

In the proposed microinverter, M_{dc1} and M_{ac} are key parameters that define its operation, and M_{dc1} varies between 0 and $1 - M_{ac}$. At the boost stage, each PV source is interfaced through a boost converter that steps up the input voltage V_{in} to the DC-link voltage V_{Cdc} . The obtained gain in this stage is determined by the modulation index M_{dc1} as shown in (6).

At the full-bridge conversion stage, the microinverter converts V_{Cdc} into an AC output voltage whose peak amplitude is governed by the modulation index M_{ac} , as

$$V_{ac,peak} = V_{Cdc} M_{ac} \quad (24)$$

By combining these two stages, the total voltage gain G_{ac} from the PV input to the AC output can be calculated as

$$G_{ac} = \frac{V_{Cdc} M_{ac}}{V_{in}} = \frac{M_{ac}}{M_{dc1}} \quad (25)$$

The dependence of the AC voltage gain G_{ac} on M_{dc1} and M_{ac} is visualized in Fig. 5. It demonstrates that, for a given value of voltage gain V_{Cdc} , it can be achieved with multiple combinations of M_{ac} and M_{dc1} along the same contour line. This endows significant flexibility to the design of modulation parameters. Obviously, the maximum AC voltage gain G_{ac} will occur at $M_{dc1} = 1 - M_{ac}$. To ensure optimal performance, it is essential to determine an appropriate M_{ac} value in prior to M_{dc1} to achieve the desired voltage gain G_{ac} and DC-link voltage. For instance, Fig. 5 indicates that both $M_{ac} = 0.8$, $M_{dc1} = 0.2$ and $M_{ac} = 0.6$, $M_{dc1} = 0.15$ can achieve the required gain of $G_{ac} = 4$. However, the first combination of $M_{ac} = 0.8$ and $M_{dc1} = 0.2$ is preferable since higher M_{ac} results in enhanced utilization of DC-bus and higher efficiency. M_{dc2} is determined by following the same principle, with the corresponding voltage gain G_{ac} . Notably, (25) here is derived by considering the negative FHC instead of the positive one. These results indicate that M_{dc1} and M_{dc2} play

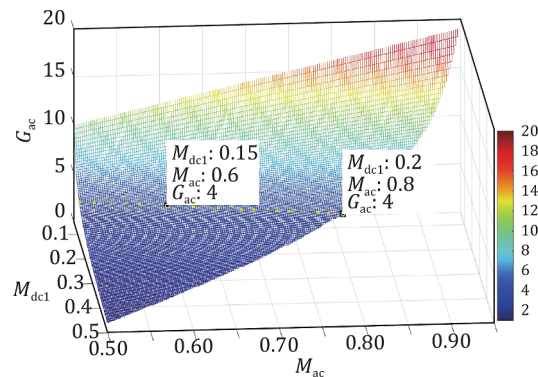


Fig. 5. Three-dimensional mesh grid of $G_{ac} = M_{ac}/M_{dc1}$ (for the dashed line, $G_{ac} = 4$). Here the numbers in the color bar (0→20) represent the voltage gain of the microinverter, which are unitless and indicate how many times the output AC voltage is amplified compared to the input DC voltage.

crucial roles in achieving efficient operation, optimized voltage gain, and improved microinverter performance.

2.3.1. Current stress of switches

It can be concluded that all four switches (S_1 – S_4) are operating under same voltage stress, which is equal to the DC-link voltage V_{Cdc} . Therefore, only the current stress these switches suffered is discussed here. As the DC-boost sub-circuit in Fig. 6(a) shows, the inductor L_2 operates in CCM, whereas the inductor L_1 transitions into DCM once the switch S_4 is turned on and the switch S_3 is turned off during the positive FHC. Thus the current through the switch S_4 is given by the difference $I_{L_2} - I_{L_1}$, and its peak value can be obtained by

$$I_{S_4,peak} = I_{L_2}^+ + \frac{V_{in2}}{2L_2}(1 - M_{dc1})T_s \quad (26)$$

When S_3 is turned on and S_4 is switched off, the same peak current flows through S_3 . Assuming the current ripple in the inductor L_1 is negligible, the root mean square (RMS) currents of S_4 and S_3 over a switching cycle can be approximated as follows:

$$I_{S_4,rms}^+ = I_{L_2}^+ \sqrt{1 - M_{dc1}} \quad (27)$$

$$I_{S_3,rms}^+ = I_{L_2}^+ \sqrt{M_{dc1}} \quad (28)$$

Similarly, a nearly identical process can be applied to calculate the RMS currents of S_3 and S_4 during the negative FHC, so it is not explicitly detailed here. Based on the current waveforms shown in Fig. 6(b), it can be deduced that, for a complete fundamental period, the RMS currents through both switches are identical and can be computed by the sum of their respective components during positive and negative FHC, as

$$I_{S_3,rms} = I_{S_4,rms} = \sqrt{(I_{S_4,rms}^+)^2 + (I_{S_3,rms}^+)^2} = I_{L_2}^+ \quad (29)$$

Accordingly, the RMS current on each switch (S_3 or S_4) in the DC-AC conversion sub-circuit of Fig. 6(a) is evaluated by

$$I_{S_{3,ac},rms} = \frac{\sqrt{2}}{2} I_{o,rms} \quad (30)$$

where $I_{o,rms}$ represents the RMS output current of the microinverter. As a result, the total current stress applied to the switches S_3 and S_4 can be evaluated by superposing the results obtained in the DC-boost and DC-AC conversion sub-circuits.

2.3.2. Power loss

As previously mentioned, two inductors, two diodes, one DC capacitor, and four switches are included in the proposed microinverter. Assuming that both inductors share the same parasitic resistance $r_L = r_{L_1} = r_{L_2}$, the conduction loss of each inductor over a fundamental period can be calculated by

$$\delta_{L_1} = \frac{1}{2}(I_{L_1}^+)^2 r_{L_1} + \frac{1}{2}(I_{L_1}^-)^2 r_{L_1} \quad (31)$$

$$\delta_{L_2} = \frac{1}{2}(I_{L_2}^+)^2 r_{L_2} + \frac{1}{2}(I_{L_2}^-)^2 r_{L_2} \quad (32)$$

During the positive FHC, L_1 is operated in DCM, with only a small average current $I_{L_1}^+$ for a short period. Consequently, the reverse current through D_1 , which is in series with L_1 , remains minimal. In the negative FHC, however, L_1 transitions to CCM, resulting in D_1 conducting continuously while no reverse-recovery loss is induced. Therefore, the reverse recovery loss by the diode D_1 can be negligible, and its conduction loss is formulated as

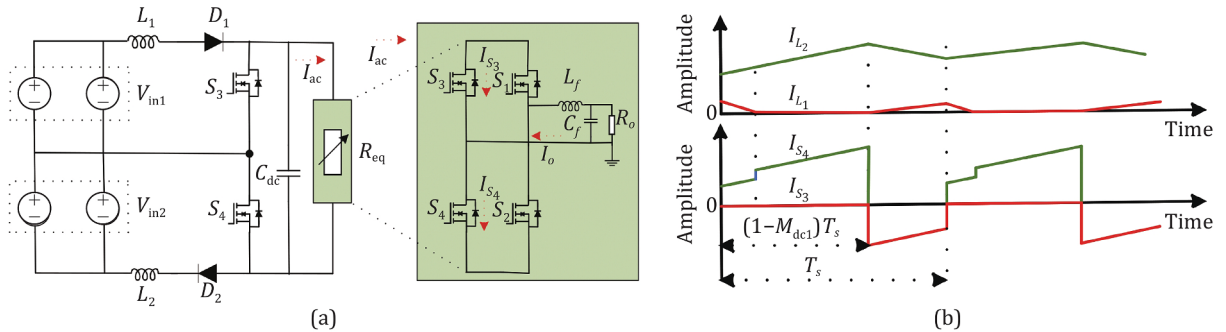


Fig. 6. Schematic diagram of current stress analysis: (a) equivalent circuit of DC-boost with DC-AC conversion and (b) current waveforms during the positive FHC of the DC-boost sub-circuit.

$$\delta_{D_1} = \frac{1}{2} \left(I_{L_1}^+ + I_{L_1}^- \right) V_F \quad (33)$$

where V_F represents the forward voltage. Similarly, the conduction loss of D_2 can be calculated by

$$\delta_{D_2} = \frac{1}{2} \left(I_{L_2}^+ + I_{L_2}^- \right) V_F \quad (34)$$

With regard to the DC-link capacitor C_{dc} , based on the current expressions shown in Table 1, its power loss across its equivalent series resistance r_c can be formulated as

$$\begin{aligned} \delta_{Cdc} = r_c f_1 \left\{ \int_0^{\frac{1}{2f_1}} \left[\left(I_{L_1}^+ \right)^2 M_{dc1} + \left(I_o - I_{L_1}^+ \right)^2 (d_1 - M_{dc1}) + \left(I_{L_1}^+ \right)^2 (1 - d_1) \right] dt \right. \\ \left. + \int_{\frac{1}{2f_1}}^{\frac{1}{f_1}} \left[\left(I_{L_1}^- \right)^2 (1 - M_{dc2}) + \left(I_{L_1}^- \right)^2 d_1 + \left(I_o - I_{L_1}^- \right)^2 (M_{dc2} - d_1) \right] dt \right\} \end{aligned} \quad (35)$$

which can be further simplified, by neglecting the contributions of $I_{L_1}^+$ and $I_{L_2}^-$ because they are far smaller than those of $I_{L_1}^-$ and $I_{L_2}^+$, as

$$\delta_{Cdc} = r_c \left(I_{L_2}^+ \right)^2 \left(1 - M_{dc1} - \frac{2M_{dc}}{\pi} \right) + r_c \frac{4V_{Cdc}^2 M_{dc}^3}{2\pi R_o^2} \quad (36)$$

The conduction loss, for each switch of H-bridge S_1 – S_4 due to respective ON-resistance R_{on} , is given by

$$\delta_{con} = I_{S_x, rms}^2 R_{on} \quad (37)$$

where $I_{S_x, rms}$ indicates the RMS current of the switch S_x , $x = 1, 2, 3, 4$. Thus, the corresponding overall switching loss is as follows:

$$\delta_{sw_x} = \frac{1}{2T_s} I_{S_x, rms} V_{Cdc} (t_r + t_f) \quad (38)$$

where t_f and t_r represent the turn-off and turn-on time of each switch, respectively. As a result, when the output power of the proposed microinverter is 1 kW, the total power loss is estimated to be 25.67 W, and the corresponding loss distribution is summarized in Fig. 7. Obviously, the losses introduced by the switches are significantly larger than those associated with the two inductors added for boosting the voltage. This means that the overall efficiency of the proposed microinverter can be enhanced by applying power switches that have low ON-state resistances R_{on} .

3. Results and discussion

3.1. Simulation

The proposed microinverter system was simulated in the MATLAB/Simulink (R2024b) software environment and the adopted key specifications are summarized in Table 2. To evaluate its feasibility for PV applications, the simulation setup included four input PV sources, each connected in parallel with a 3.3-mF capacitor for filtering. All these four PV sources were modeled with identical characteristics as shown in Fig. 8, where the maximum power point (MPP) is clearly visible. Then MPP tracking was performed by adjusting the modulation indices M_{dc1} and M_{dc2} , which in turn changes the average inductor currents I_{L_1} and I_{L_2} .

Fig. 9(a) presents the simulated results of several key waveforms related to the microinverter performance. Obviously, a double line-frequency ripple appears in the DC-link voltage (V_{Cdc}). This is mainly because that most of the oscillating single-phase output power is absorbed by the capacitor. As a result, minimal ripple power is reflected to the PV sources. Moreover, small ripples are observed in both PV voltages and currents, which are primarily due to the alternating operation between CCM and DCM, governed by the MPWM strategy. However, the resulted output power waveforms illustrated in Fig. 9(b) demonstrate that, the four included PV sources consistently deliver stable maximum power throughout the cycle despite these fluctuations.

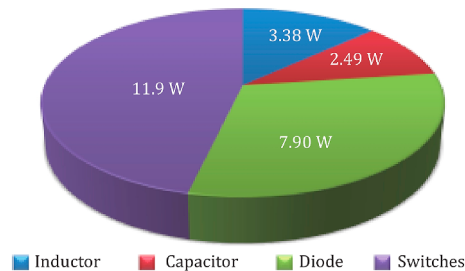


Fig. 7. Estimated loss distribution of the proposed microinverter.

Table 2
Microinverter specifications.

Parameter	Specification
Input DC voltage	70 V
Output AC voltage (V_o)	220 V, 1 kW
Modulation index	$M_{ac} = 0.8$; $M_{dc1} = 0.17$
Carrier frequency (kHz)	30
Inductors (μ H)	450
DC-link capacitor (μ F)	440
Diodes	FFSH1665A
Power switches	TP65H150G4PS (650 V, $R_{on} = 180$ m Ω)

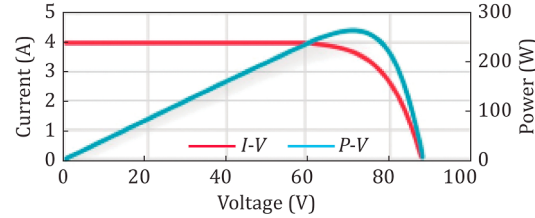


Fig. 8. Simulated PV characteristics.

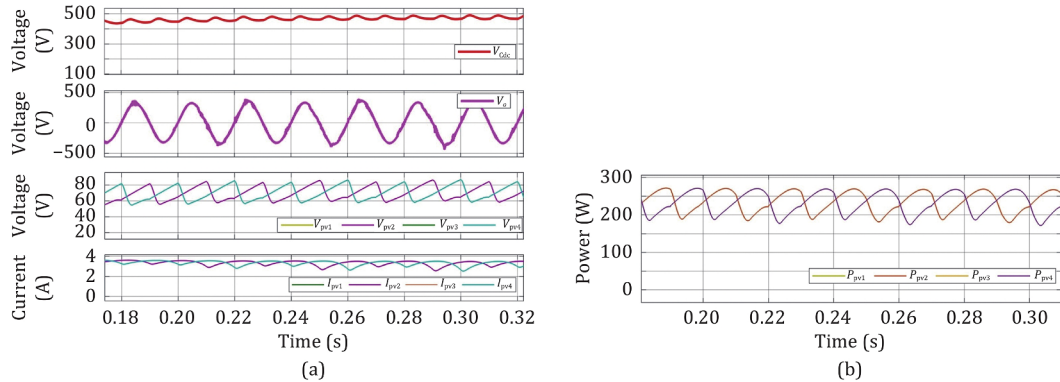


Fig. 9. Simulated waveforms of (a) DC-link voltage, output voltage, and the voltages and currents of each included PV source; (b) output power of each PV source. Notably, the waveforms of voltage, current, and power for the four PV sources overlap due to their identical characteristics and operation conditions, and thus only two curves can be visibly distinguishable.

3.2. Experiment

To experimentally validate the performance of the proposed microinverter and the feasibility of the control strategy, a 1-kW GaN-based single-phase microinverter was constructed and tested. The experimental setup, as shown in Fig. 10, was assembled based on the specifications listed in Table 2. The prototype was controlled by a digital signal processor (DSP) TMS320F28379D and powered by four independent DC power supplies (EA-PS 9080-100) to emulate PV sources. Its output was connected with resistive loads. The experimental waveforms were recorded by an oscilloscope (Tektronix MDO3024). The voltage waveforms were measured by a voltage probe (SI9002), and current waveforms were measured by a current probe (SRS6150) with 50-MHz bandwidth.

3.2.1. Steady-state performance

When the DC inputs of $V_{pv1} = V_{pv2} = V_{in1} = 70$ V and $V_{pv3} = V_{pv4} = V_{in2} = 70$ V, as detailed in Table 2, are applied, the measured waveforms of the inductors' currents, output voltage, and DC-link voltage are shown in Fig. 11, with the DC-link voltage of 400 V and the output AC voltage of 220 V. Correspondingly, the voltage gain is calculated to be 4.2. It can be observed that the 440- μ F DC-link capacitor exhibits a stable average voltage. Although it is accompanied by a slight ripple at twice the line frequency, this is the typical characteristic of single-phase systems. The current waveforms also confirm that the two inductors alternate between CCM and DCM without overlapping. This behavior remains consistent, even near the zero-crossings of the fundamental cycle, as highlighted in the red-boxed region. Moreover, during DCM operation, the peak currents through the inductors remain quite low, which demonstrates that the conduction losses are minimized.

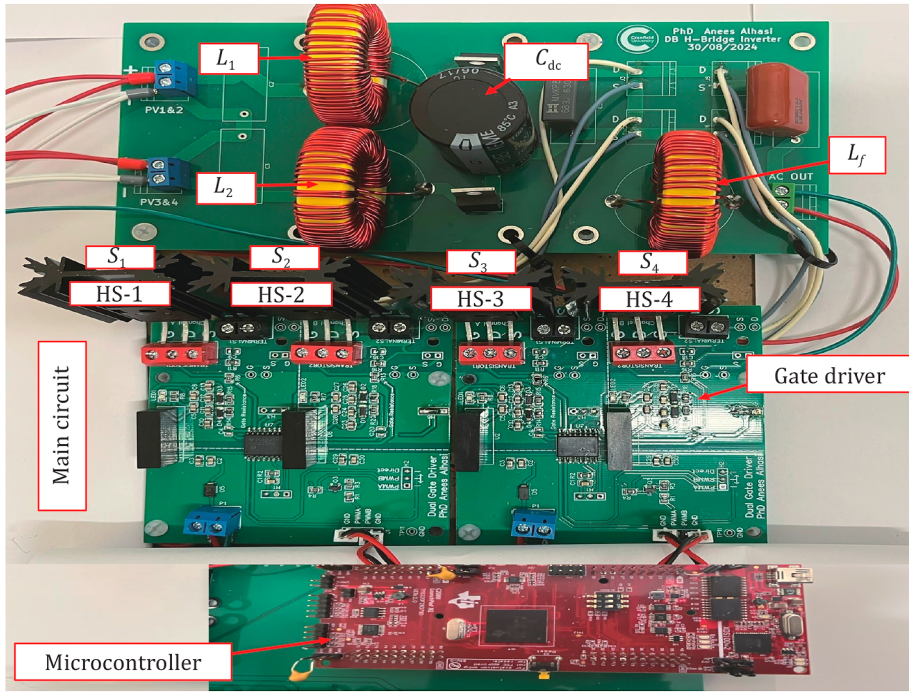


Fig. 10. Experimental prototype of the proposed microinverter. Here HS-1, HS-2, HS-3, and HS-4 denote the heat sinks of switches S_1 – S_4 , respectively.

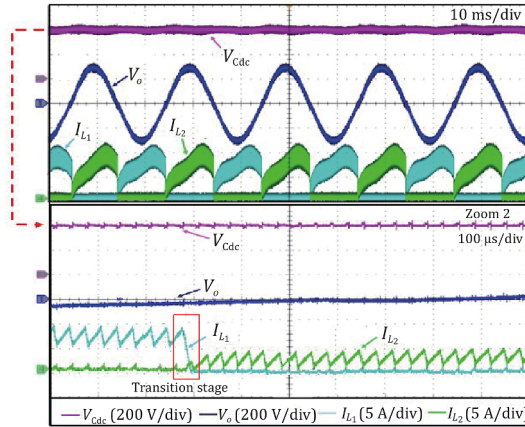


Fig. 11. Measured waveforms of the inductors' currents, output voltage, and DC-link voltage of the proposed microinverter.

It is also demonstrated that stable performance can be obtained even when the proposed microinverter is subjected to unequal input voltages. Taking the input voltages of $V_{pv1} = 50$ V, $V_{pv3} = 70$ V and $V_{pv2} = 60$ V, $V_{pv4} = 80$ V under full-load operation as examples, the output waveforms of the proposed microinverter are illustrated in Figs. 12(a) and (b), respectively, with appropriately selected modulation indices M_{dc1} and M_{dc2} . This means that the microinverter continues to operate reliably once the modulation indices M_{dc1} and M_{dc2} were deliberately determined based on (6) and (7) to maintain a constant DC-link voltage. When the input voltages of V_{pv1} , V_{pv2} , and V_{pv3} are reduced to zero, the single-boost (SB) mode is activated and the corresponding results are shown in Fig. 12(c). In this scenario, a slight increase in the DC-link voltage ripple is observed compared to that of the DB mode. This is primarily due to the absence of energy input from V_{in1} during the negative FHC. Despite this, a steady DC-link voltage can still be maintained by adopting an appropriate DC-link capacitor C_{dc} , as suggested by (8).

3.2.2. Dynamic performance

To investigate the dynamic performance of the proposed microinverter, its output response under abnormal operation conditions was studied. During the experiment, the input PV source V_{pv3} was temporarily deactivated to simulate the transition into the SB mode

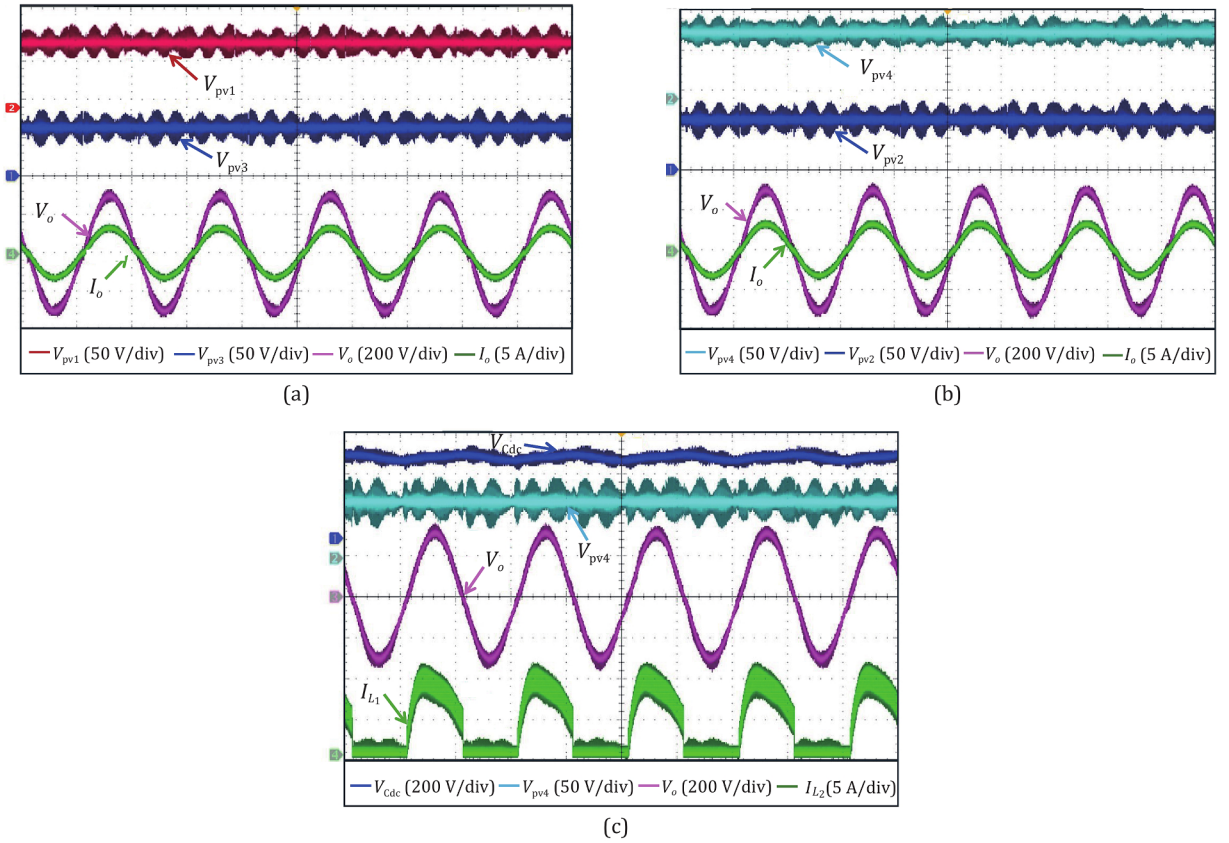


Fig. 12. Experimental waveforms of the proposed microinverter: (a) $V_{pv2} = 0.70V_{pv4}$, (b) $V_{pv1} = 0.73V_{pv3}$, and (c) $V_{pv1} = V_{pv2} = V_{pv3} = 0$.

and then reactivated to return to the DB mode. These obtained results as shown in Fig. 13 confirm the proposed microinverter's ability to perform mode transitions smoothly while no system stability is sacrificed. For example, when V_{pv3} is subjected to a sudden drop from its rated value to zero, a complete shading or open-circuit fault can be simulated. The corresponding experimental results are shown in Fig. 13(a). It is obvious that both the measured output voltage V_o and output current I_o exhibit stable and undistorted sinusoidal waveforms, despite this abrupt change occurred. This demonstrates the microinverter is capable of continuing delivering power from the remaining three PV inputs without interruption. It also validates the robustness of its control strategy and fault tolerance of its multi-input design. By reversing the input V_{pv3} to emulate a fault condition or misconnection, the measured results are shown in Fig. 13(b). No noticeable degradation is observed in the output response, which further indicates its strong fault tolerance. Meanwhile, both V_o and I_o waveforms have a sinusoidal nature and amplitudes close to their rated values. It indicates that the proposed microinverter can isolate or reject the faulted input and simultaneously sustain regulated power delivery to the load. In brief, the proposed microinverter is capable of operating steadily not only when one of its PV sources fails but also it is reversed. This makes it well-suited

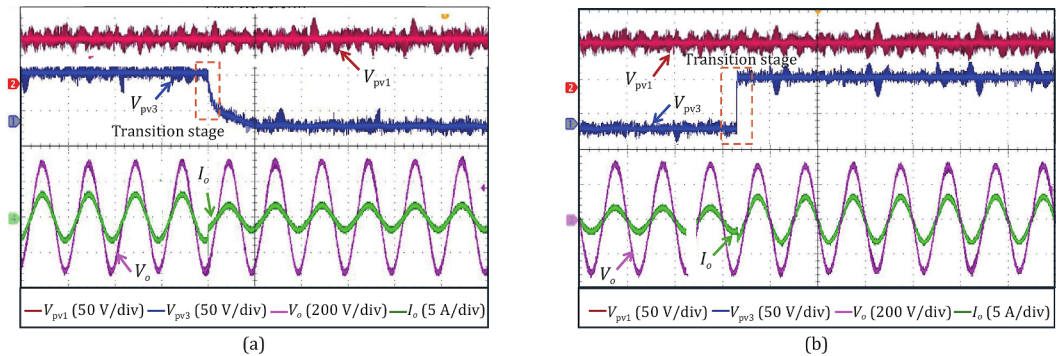


Fig. 13. Dynamic response of the proposed microinverter to abnormal input conditions with V_{pv3} (a) dropping to zero and (b) reversing.

for real-world PV installations where mismatch and shading are usually happened.

To demonstrate the generalizability of the designed control strategy in the proposed microinverter, non-ideal load conditions including capacitive and inductive loads are considered. Fig. 14(a) shows the output results of the proposed microinverter subjected to a capacitive load consisting of a $100\text{-}\Omega$ resistor connected in parallel with a $50\text{-}\mu\text{F}$ capacitor ($100\text{ }\Omega + 50\text{ }\mu\text{F}$). In this condition, the output current I_o leads the output voltage V_o , indicating a leading power factor. For an inductive load formed by a $100\text{-}\Omega$ resistor in series with a 50-mH inductor ($100\text{ }\Omega + 50\text{ mH}$), the results in Fig. 14(b) show that the current waveform slightly lags behind that of the voltage. As expected, it confirms the typical behavior of a lagging power factor. Obviously, all the measured results under both capacitive-load and inductive-load conditions exhibit stable and clean sinusoidal waveforms even though additional phase shifts are introduced. That is to say, the proposed microinverter can operate steadily when the loads are supplied with different power factors. Despite this phase shift, both voltage and current waveforms remain sinusoidal, showing that the proposed microinverter can handle reactive loads without degrading waveform quality. It is also demonstrated that the proposed microinverter exhibits low output impedance and inherent ability to prevent waveform distortion under different load conditions. As a result, it can be inferred that the proposed microinverter is able to perform reliably and efficiently under various practical load conditions, especially in these environments with non-unity power factors.

The dynamic performance of the proposed microinverter considering the abrupt changes in input power is studied. Fig. 15(a) is obtained when the input power is gradually reduced to 50% of its rated value, and Fig. 15(b) corresponds to that the input power is recovered from 50% to 100%. They reveal that these abrupt changes nearly have no influence on the output voltage (V_o) waveform, exhibiting excellent voltage regulation performance. However, the output current (I_o) and the combined input current $I_{L1} + I_{L2}$ are changed accordingly to accommodate the variations of input power. These results further confirm the robustness of the proposed microinverter and its adaptability to large input fluctuations, which is typically existed in renewable energy sources.

When a 30% sag is programmed in the output voltage (V_o) and lasts for ten cycles before recovering to its pre-sag value, the resulted dynamic response is exhibited in Fig. 16. During this sag period, a corresponding rise is observed in the amplitude of the output current (I_o) waveform. This increase contributes to constant output power despite the reduced voltage. Once the voltage is recovered to its nominal value, the current promptly returns to its original level, indicating the efficient power regulation achieved by the control strategy proposed in the microinverter. In addition, the smooth and stable response further demonstrates its resilience against grid voltage disturbances.

Fig. 17 compares the simulated and experimental efficiency results of the proposed microinverter with output power increasing

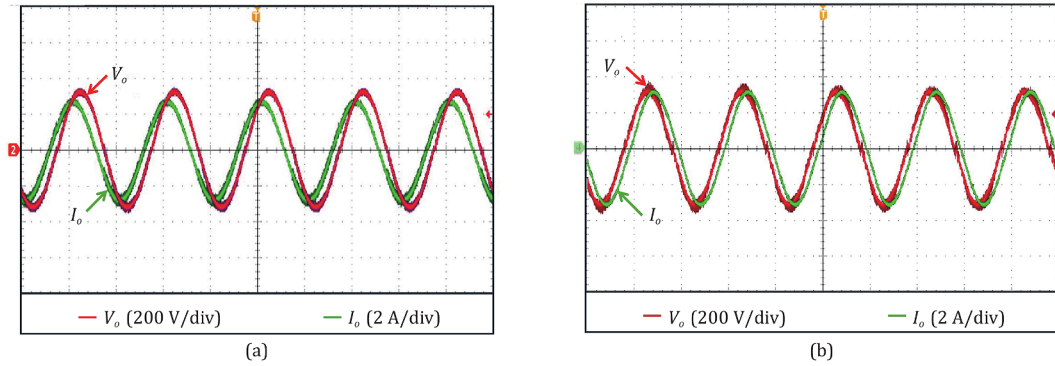


Fig. 14. Experimental results of the proposed microinverter under different load types: (a) capacitive load exhibiting a leading power factor and (b) inductive load exhibiting a lagging power factor.

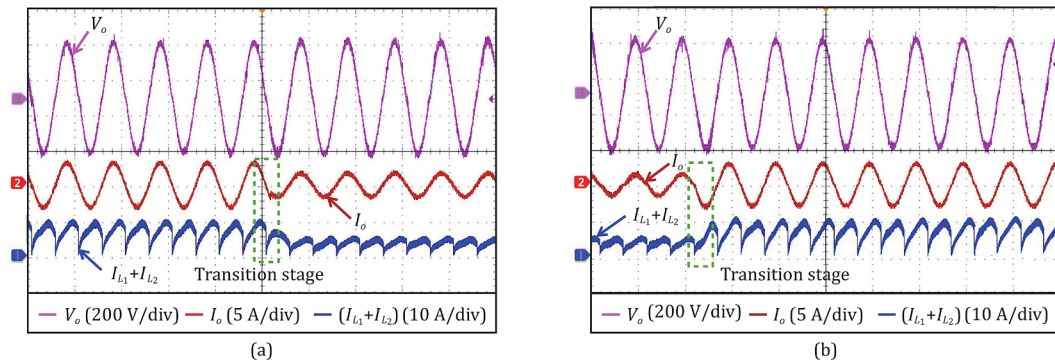


Fig. 15. Experimental results of the proposed microinverter with abruptly changed input power: (a) reducing from 100% to 50% and (b) recovering from 50% to 100% of its rated value.

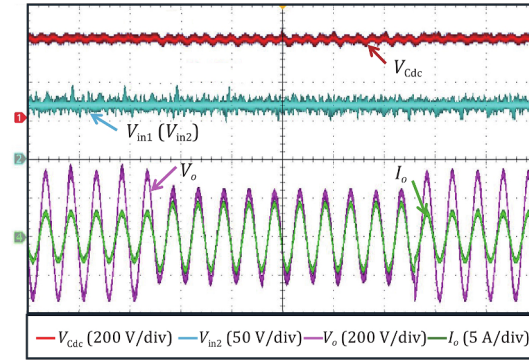


Fig. 16. Experimental results when a 30% sag is introduced in the output voltage.

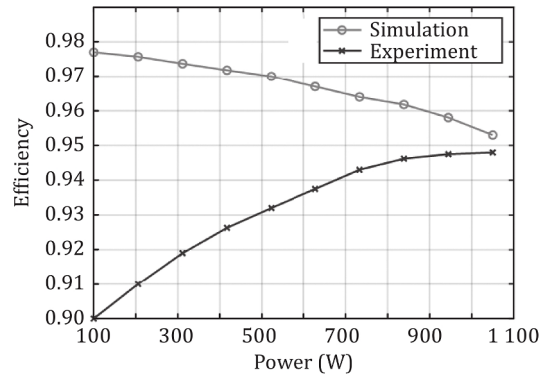


Fig. 17. Simulated and experimental efficiency of the proposed microinverter as a function of output power.

from 100 W to 1 kW. The simulated efficiency is gradually decreased from its peak value of approximately 97.8% to around 95.3% at the full load, and the experimental one is increased from 90% to about 94.8% at the full load. Obviously, the largest difference between the simulated and experimental results is generated at light-load conditions, i.e., low output power ranges. This is mainly because that the fixed losses, such as driver and auxiliary circuit consumption, are not fully taken into account in the simulation model, which assumes an ideal or simplified component behavior. As we all know, in power electronic systems, these losses become more dominant at low output power. Even so, the deviation between simulated and experimental efficiency is tolerable, and the negative impact induced by these omitted fixed losses becomes weaker as the output power increases, finally resulting in an extremely small difference of 0.7% at the full load. The largest efficiency of approximately 94.8% is measured at rated power during the experiment, which is larger than that reported in Refs. [19,22,25,28]. This further demonstrates the feasibility and superiority of the proposed design in practical applications.

3.2.3. Comparison with advanced single-phase transformerless microinverters

Table 3 compares our proposed microinverter with the existing single-phase transformerless microinverters. It shows that the total components used in the proposed microinverter are relatively less. Especially for the active switches, the required number of our design is the least. Even though an equivalent amount of switches is adopted by Xiao et al. [28], more diodes and capacitors should be included. This indicates that our proposed microinverter has more advantages over other existing counterparts in terms of system complexity and cost. Moreover, even compared with other traditional designs, it is still superior. For example, the five-switch dual-input transformerless microinverter presented in Ref. [25] also offers high voltage gain and supports unbalanced input sources. However, it is an off-grid solution, which requires high-capacitance input-side capacitors. Although such high-capacitance capacitors are also used in our design, they can be replaced by long-life, low-capacity film capacitors through active power decoupling which cannot be implemented in Refs. [19,22,25]. Because a common-ground structure between the input and output is applied in our proposed microinverter to effectively eliminate the CM leakage current. This contributes to a reduction in both active and passive components and benefits to enhance efficiency and reliability of the overall system. It is also worthy to note that although all referenced microinverters [19,22,25,28] operate with similar voltage ratings, their capacitors intended to absorb second-order power oscillations, which are typically existed in single-phase systems, are usually situated close to the PV sources at reduced voltage levels, necessitating larger capacitance values. Additionally, their voltage gain is relatively low, limiting their suitability for integration with low-voltage PV sources. Briefly, the proposed microinverter operates at a lower switching frequency and achieves competitive efficiency while requiring fewer switching devices. Based on a standard H-bridge with integrated DB functionality, it can offer a high

Table 3

Comparison of the proposed microinverter with the existing advanced single-stage transformerless microinverters.

Topology	[19]	[22]	[25]	[28]	Proposed in this paper
Number of PV sources	2	2	2	2	1, 2, 3, or 4
Type of devices	Si	Si	Si	SiC	GaN
Number of switches	6	12	5	4	4
Number of diodes	0	0	1	4	2
Number of inductors	1	2	2	2	2
Inductance of each inductor (mH)	0.4	1.2	0.1	3.6	0.45
Number of capacitors	1	3	2	2	1
Capacitance of each capacitor (μF)	6.8	470	200	50	440
Voltage stress of switches	$S_1, S_2 : 2V_{\text{Cdc}}$ $S_3, S_4 : V_{\text{Cdc}}$ $S_5, S_6 : V_{\text{ac}}$	$S_1, S_2 : V_{\text{Cdc}}$ $S_3 - S_6 : 3V_{\text{Cdc}}$ $S_{k1} - S_{k3} : V_{\text{Cdc}}$	$S_1 - S_4 : > V_{\text{ac}}$ $S_5 : > 2V_{\text{ac}}$	$S_1, S_3 : > 2V_{\text{ac}}$ $S_2, S_4 : > V_{\text{ac}}$	$S_1 - S_4 : V_{\text{Cdc}}$
Current stress of switches	$S_1 - S_6 : > I_{\text{ac}}$	$S_1, S_2 : I_{\text{ac}} + I_{\text{pv}}$ $S_3 - S_6 : I_{\text{pv}}$ $S_{k1} - S_{k3} : 2I_{\text{pv}}/3$	$S_1 : I_{L1}$ $S_2, S_3 : I_{L2} + I_g$ $S_4, S_5 : I_g$	$S_1 - S_4 : I_{\text{pv}}$	$S_1, S_2 : I_{\text{ac}}$ $S_3, S_4 : I_{\text{ac}} + I_{L2}$
Dual grounding	No	No	Yes	Yes	Yes
Power decoupling	Inherent	E-cap	E-cap	Inherent	E-cap
Voltage gain G_{ac}	2.2	5	2.6	8.1	4.2
$V_{\text{in}} \rightarrow V_o$ (V)	85→170	30→110	54→110	36→110	70→220
Frequency (kHz)	30	$f_{\text{dc}} = 20; f_{\text{inv}} = 10$	20	20	30
Efficiency	94.3%	91%	94.6%	94.6%	94.8%
Operation	CCM	CCM	DCM	CCM	CCM/DCM
Rated power (W)	400	300	250	400	1000

voltage gain level by deliberately determining the modulation index.

While it has been demonstrated that our proposed topology can operate stably under varying input conditions, some limitations are still existing. When it operates in DCM, particularly under relatively low input voltages, the current ripple may be increased and additional stress may be imposed on the inductors compared to that in CCM. Therefore, delicately-designed inductors are required to maintain high efficiency and reliability under extreme conditions. Furthermore, although the proposed microinverter supports multiple PV inputs, scalability to a larger number of sources is still challenging in terms of control coordination and thermal management. The efficiency decrease at the light load as shown in Fig. 13, which is primarily induced by fixed driver and auxiliary losses dominating at low power, also remains to be solved. These issues may be mitigated by further optimizing the driver circuit and adaptive switching schemes.

4. Conclusions

This paper proposed a novel single-phase, non-isolated, multi-input microinverter for PV applications, which connects PV sources to the grid through a shared DC and AC ground, thereby eliminating the CM leakage current without requiring additional active components. It employs only four switches to support up to four PV panels. By further incorporating a simplified carrier-based modulation strategy with modified reference signals to stabilize the DC-link voltage while minimizing the low-frequency current ripple, the proposed topology achieves high voltage gain in a single-stage structure. These designs collectively reduce the conduction losses, lower the current stress on switches and diodes, and enhance the overall system's efficiency and reliability. Furthermore, the microinverter demonstrates robust performance under shaded and unbalanced PV input conditions. It can continuously deliver power even when one or more sources are compromised. The system was experimentally validated through a 1-kW hardware prototype, confirming its feasibility and applicability in real-world PV systems. Aiming at higher power ratings, we will try to integrate wide-bandgap semiconductor devices to further improve efficiency and power density, develop advanced control algorithms to enhance dynamic performance under rapidly changing solar and load conditions, and incorporate grid-support functionalities such as reactive power control, fault ride-through capability, and compliance with evolving grid codes in our future work. All of these may position the proposed microinverter as a strong candidate for next-generation PV power conversion systems.

CRedit authorship contribution statement

Anees Alhasi: Conceptualization, Methodology, Mathematical modeling, Simulation, Writing–original draft, Visualization, Formal analysis, Data curation. **Patrick Chi-Kwong Luk:** Supervision, Validation, Writing–review & editing, Project administration, Funding acquisition, Conceptualization. **Khalifa Aliyu Ibrahim:** Investigation, Simulation, Resources, Writing–review & editing, Data curation. **Zhenhua Luo:** Validation, Resources, Formal analysis, Writing–review & editing.

Declaration of competing interest

The author declares that there is no conflict of interest regarding the publication of this paper.

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