Robust Synchronized Data Acquisition for Biometric Authentication

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***Abstract*—Owing to its unique, concealment and easy customization by combining different wrist and hand gestures, high-density surface electromyogram (HD-sEMG) is recognized as a potential solution to the next generation biometric authentication, which usually adopts a wireless body sensor network (BSN) to acquire the multi-channel HD-sEMG biosignals from distributed electrode arrays. For more accurate and reliable classification, biometric authentication requires the distributed biosignals to be sampled simultaneously and be well aligned, which means that the sampling jitters among the arrays need to be tiny. To synchronize data sampling clocks of a cluster of BSN nodes for biometric authentication, this article modifies the packet-coupled oscillators protocol by using a dynamic controller (D-PkCOs). This protocol only involves one-way single packet exchange, which reduces the communication overhead significantly. For the purpose of maintaining precise sampling of these BSN nodes subject to drifting clock frequency and varying delays, the dynamic controller is designed via the H_∞ robust method, and it is proved that all the BSN nodes' sampling jitters are bounded. The experimental results demonstrate that the D-PkCOs protocol can keep the sampling jitters less than a microsecond in a 10-node IEEE 802.15.4 network. The application of D-PkCOs to the BSN shows that the HD-sEMG signal with a high signal-to-noise ratio is obtained, which leads to better gesture classification performance.**

***Index Terms*—Clock synchronization, H_∞ control, packet-coupled oscillators (PkCOs).**

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I. Introduction

THANKS to the unique and difficult-to-manipulate attributes of biometric traits [1], they are widely used in many applications (e.g., border control [1], biometric cash machine [2], and smart healthcare [3]) for reliable authentication or identification. Over the last decade, due to the rapid advancements of sensor technology and artificial intelligence (AI), traditional biometric authentication, such as fingerprint verification or facial recognition, has become vulnerable. For instance, fingerprints can be acquired by any touched surface or be forged with plastic molds, and facial characteristics are able to be captured via high-resolution photography or be synthesized by AI [4].

Fortunately, utilizing electrical biosignals as biometric traits can overcome the abovementioned drawbacks, and both electrocardiogram (ECG) and electroencephalogram (EEG) signals have been popular solutions. However, the ECG signal is sensitive to heart rate variations caused by physiological and emotional factors. EEG's low signal-to-noise ratio (SNR) and complex signal sampling process also limit its application [5]. By contrast, the surface electromyogram (sEMG) biosignal has been well applied in the human–machine interface (e.g., Myo [6] and Pre-fall Detection System [7]), owing to its higher SNR [8] and convenient sEMG data acquisition procedure. Also, the sEMG signal customized by combining different wrist and hand gestures provides a better level of protection. Several recent works (e.g., [1] and [5]) demonstrate that the high-density sEMG (HD-sEMG) signal can be used as a biometric trait, and enhance the reliability of a biometric system.

Typically, multiple (e.g., 4 in [9]) electrode arrays are used to obtain the HD-sEMG signals for authentication. However, the existence of cable connections among these electrode arrays poses challenges for signal recording in dynamic environments. Hence, Cerone [10] developed a wireless HD-sEMG detection system, and all the arrays, which constitute a body sensor network (BSN), are communicated wirelessly. To ensure that the distributed HD-sEMG signals are well aligned for accurate

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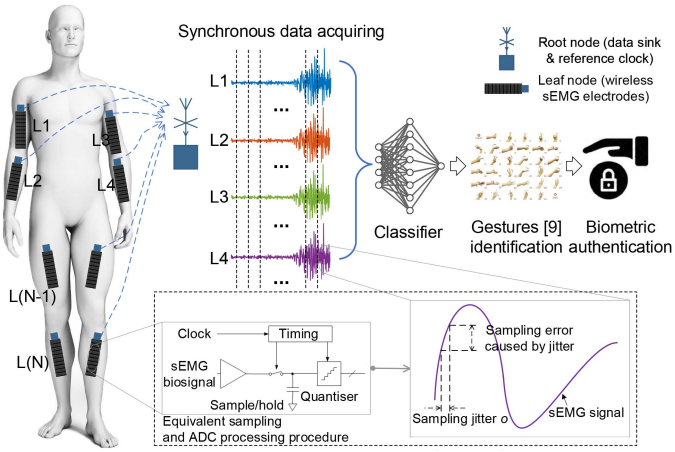

Fig. 1. Synchronous HD-sEMG sampling for biometric authentication.

gesture classification, it is essential to let the data sampling progress be synchronous among electrode arrays [10], [11].

In Fig. 1, if no synchronization technique is utilized, data sampling clocks, which provide the timing signal to the sample/hold function of analog-to-digital converters (ADC) components, will be poorly synchronized. Variations in the sampling time (referred to as the sampling jitters) among the electrode arrays let the sampling instants vary from each other. This transfers the sampling jitters from the clocks to the sampled HD-sEMG signals. The sampling errors caused by the jitters let the (distributed and sampled) biosignals be poor aligned, which reduces the gesture classification accuracy and authentication system performance. The key enabling technology of synchronization can achieve such a goal (i.e., synchronizing data acquiring clocks in a BSN) [12], and this work modifies the packet-coupled oscillators (PkCOs) protocol by using a dynamic controller (D-PkCOs). We also use the H_∞ control solution to guide the parameter selection of the dynamic controller, thereby allowing the sampling jitters of all the data acquiring clocks are bounded. This also represents that the sampling errors are limited. Hence, the wireless electrode arrays can obtain the HD-sEMG biosignals simultaneously, and the high gesture classification accuracy is also guaranteed.

A. Related Work

Due to the characteristics (e.g., reliability and low energy consumption) of single-hop single-cluster topology, it has been a popular solution for a body sensor network. Instead of adopting an external hardware synchronization unit (e.g., [10]), we utilize a synchronization protocol for synchronizing data acquiring clocks in the BSN. The D-PkCOs algorithm is on the medium access control (MAC) layer; no additional hardware design is required.

Until now, several communities have extensively studied the topic of synchronization, owing to its significance. In the early works of clock synchronization, the main focus is on how a wireless network can realize higher synchronization precision via the packet exchange strategy. One solution is the one (or two)-way sender to receiver algorithm, e.g., timing-sync protocol for sensor networks (TPSN) [13]. The other is the receiver to receiver synchronization protocol, and a famous example is reference broadcast synchronization [14]. However, these protocols transmit numerous packets (e.g., 100 in [15]) during each synchronization cycle T. The frequent radio frequency (RF) communication puts a strain on the battery-powered BSN node. The D-PkCOs algorithm only needs to send one packet (i.e., Sync) in T, this solution reduces the communication overhead.

Even though the standard deviation of MAC-level timestamp accuracy is around 1 μs [16], within the progress of sending and receiving a packet, the use of two timestamps for calculating clock offset[1] still lets the one-way synchronization protocol [on the high-frequency (e.g., 32.768 MHz) embedded clock] suffer from the timestamp accuracy. In this work, the adopted D-PkCOs algorithm only requires one timestamp, which is generated on the receiver's reception of the Sync packet. Sync itself contains the timing information (i.e., clock's resetting). Therefore, compared with the one-way sender to receiver algorithm, D-PkCOs decreases the impacts from the timestamp uncertainty.

The synchronization performance not only can be enhanced via the packet exchange strategy, but also be improved by using advanced processing technologies. It is well known that the clock frequency needs to be adjusted to maintain the longer synchronized state; otherwise, the existence of clock skew[2] leads to more frequent packet exchange and clock correction action [17], [18]. Thus, recent works adopt multiple solutions (e.g., maximum likelihood estimation [15], [19], and linear least squares regression [20]) to estimate a more accurate clock skew for correction. However, these two methods need considerable computational overhead [21], [22], and the required time for calculating the skew estimate (i.e., processing delay) also varies in different (i.e., single precision or double precision) floating-point formats [22]. Moreover, the use of a limited number (e.g., 5 in [15]) of timestamps reduces computing accuracy [20]. Thus, the calculation of linear least squares regression moves to the cluster head with adequate computing resources [20], or is implemented via field-programmable gate array (FPGA) [21].

The use of the constant adjustment amount also is an alternative solution for clock frequency correction, while such a strategy (i.e., no varying and low-resolution correction value) limits synchronization performance [12], [23]. Hence, a proportional (P) controller [16] is utilized to solve the abovementioned issue. In [21], the moving average solution is adopted for clock skew estimation, and a proportional–integral (PI) controller is used in [12] for eliminating the impacts of drifting clock skew. Furthermore, the results of [24] and [25] show that applying the PI controller on clock offset adjustment can automatically remove the effects of varying processing delay; however, no skew correction input is employed to the local clock in these two works. Hence, we use a dynamic controller (which is an advanced version of the PI controller and moving average

[1]Offset is referred to as the time difference between two clocks.

[2]Skew is defined as the normalized difference between two drifting clock frequencies, see (4) of Section II.

methods) to adjust both the clock offset and skew, thereby extending previous works (i.e., [16], [24], and [25]). This recursive controlling strategy possesses the features of compensating for the impacts of drifting clock frequency, and naturally removing the effects of varying processing delay.

In addition, although the abovementioned works consider the consequences of drifting clock frequency, only the theoretical analysis of synchronization protocols is presented (e.g., [21], [24], [25], and [26]). This means that parameters (e.g., of the PI controller and moving average solutions) are determined empirically [12], [21]. In [16], the H_∞ method is used to design the P controller parameters in a pairwise network. Nevertheless, this work utilizes the H_∞ solution for networked dynamic controller parameters' selection. From the viewpoint of a body sensor network (i.e., a single-hop single-cluster topology), the ratio between the modulus of the sampling jitters (which indeed are the synchronization precision) and the magnitude of the noises (consisting of the drifting clock, varying processing delay, and timestamp noises) is always less than a given value. Thus, the sampling jitters of all the wireless nodes are bounded, and the sampling errors of sampled HD-sEMG signals are also limited.

Inspired by the success of various types of neural networks (NNs) in tackling handwritten digits recognition and image classification problems, recently, NN-based hand gesture classification has attracted growing attention. For example, the convolutional neural network (CNN) has been widely used for hand gesture classification, where the image [27], radar data [28], and HD-sEMG signal [29] are used as input features for training, validation, and test. So far, there exists no consensus on the optimal NN architecture [9]. Thus, in this article, we use another technique, namely, linear discriminant analysis (LDA), for studying the application of D-PkCOs in hand gesture classification.

B. Contribution and Article Organization

This work uses a D-PkCOs protocol to synchronize data sampling clocks in a body sensor network, thereby realizing simultaneous signal recording among distributed electrode arrays. Instead of adopting an external hardware unit to achieve such a goal, the adopted synchronization algorithm is on the MAC layer, and no additional hardware design is needed. The D-PkCOs protocol only requires one Sync packet during each cycle T, which reduces the communication overhead.

To realize precise sampling of all BSN nodes subject to the drifting clock frequency and varying processing delay, we adopt a dynamic controller to correct both the clock offset and skew for reducing the sampling jitters. This solution possesses the benefits of automatically removing the effects of varying processing delay, and estimating a more accurate clock skew for adjustment. In addition, we also use the H_∞ control method to design parameters of the D-PkCOs synchronization protocol. Hence, the ratio between the modulus of the sampling jitters and the magnitude of the noises is always less than a given value. This means that, in the BSN, the drifting clock and varying processing delay possess a tiny impact on the sampling jitters. Thus, the sampling errors of the HD-sEMG biosignals are also limited. The experimental results demonstrate that our D-PkCOs protocol can keep the sampling jitters less than a microsecond in a 10-node IEEE 802.15.4 network. The application of D-PkCOs to the BSN shows that the HD-sEMG signal with a high SNR value is obtained, which leads to a small gesture classification error rate.

The rest of this article is organized as follows: Section II presents the problem formulation and drifting clock model. Then, Section III shows the dynamic packet-coupled synchronization scheme, and the H_∞ design for the dynamic controller of D-PkCOs is presented in Section IV. Section V demonstrates the simulation and experimental evaluation of the D-PkCOs protocol. The application of the adopted synchronization algorithm to a HD-sEMG-based authentication system is included in Section VI. Finally, Section VII concludes this article.

II. Problem Formulation and Clock Model

This section first relates the synchronized HD-sEMG biosignal acquisition problem to the issue of synchronization on the sampling clocks, in order to define the task of this work. Next, we derive a drifting clock model for applying a dynamic controller and the H_∞ control to reduce the sampling jitters in the later section.

A. Problem Description

In the body sensor network, if no (or poor) synchronization is applied to the data sampling clocks, all the ADC switches will be opened at different sampling time (see Fig. 1), which means that all the sensor nodes cannot simultaneously acquire the biosignals. Thus, the sampling jitters on the clocks lead to sampling errors (i.e., error voltages), and these error voltages are proportional to the magnitude of the jitters and the signal slew rate, as shown in Fig. 1. Furthermore, the maximum SNR value of the sampled biosignals is determined by the amount of the jitters [30] as follows:

$$\mathrm{SNR} = -20\log(2\pi f_{\mathrm{in}} o) \tag{1}$$

where f_{in} is the input HD-sEMG signal frequency, and o is the jitter in root mean square seconds. From (1), it can be seen that the smaller jitter o results in a better sampled signal with higher SNR. The high-quality sampled HD-sEMG signals can let us obtain the trained classifier with a better gesture identification classification rate.

Thus, this work aims to use the D-PkCOs protocol to synchronize all the local data sampling clocks, and reduce the jitters, which are subject to drifting clock frequency and varying delays. Once the sampling jitters is kept as small as possible, according to (1), the BSN can obtain the good-quality HD-sEMG signal with a high SNR value. In the following, we derive an analytical model to describe the jitter o in (1), since it provides a simpler approach when the H_∞ control solution is employed to design the dynamic controller parameters, and to make the sampling jitters tiny.

B. Drifting Clock Model

Given a directed single-hop single-cluster BSN described by the digraph $\mathcal{G} = (\mathcal{V}, \mathcal{E}, \mathcal{A})$, where $\mathcal{V} = \{0, 1, \ldots, N\}$ denotes a set of nodes, and a set of edges $\mathcal{E}$ induced by the adjacency matrix $\mathcal{A} = [a_{ij}] \in \mathbb{R}^{(N+1)\times(N+1)}$. The wireless network is composed of a root node (i.e., $i = 0$) and a set of leaf nodes represented by $\mathcal{N} = \{i : i \in \mathcal{V}, \text{and } i \geq 1\}$ (see Fig. 1). The root node is unique, and also is equipped with a global positioning system (GPS) clock to provide the reference time to all the leaf nodes. If the ith leaf node can receive the Sync packet from the root node, the weight a_{i0} is one (i.e., $a_{i0} = 1$ and $a_{i0} \neq a_{0i}$); otherwise, it equals zero. In addition, the digraph $\mathcal{G}$ has no self-loop (i.e., $a_{ii} = 0$ for all $i \in \mathcal{V}$), owing to the inherent feature of RF communication. The in-degree of node i is defined as $\deg_i = \sum_{j=0}^{N} a_{ij}$. The Laplacian matrix $\mathcal{L} = [l_{ij}] \in \mathbb{R}^{(N+1)\times(N+1)}$ of $\mathcal{G}$ is represented by $\mathcal{L} = \mathcal{D} - \mathcal{A}$, where $\mathcal{D} = \text{diag}(\deg_0, \deg_1, \ldots, \deg_N)$ is the diagonal matrix.

Typically, the clock module of a sensor node consists of 1) a hardware oscillator ticking at the nominal frequency $f_0 = 1/\tau_0$, where τ_0 is the nominal clock period, 2) and a counter register, counting the number of ticks generated by the hardware oscillator. Each time the counter register matches the threshold value φ_0, it is reset to 0, and restarts counting from zero. The time variable $P_0[n]$ is introduced to model the dynamics of such an ideal hardware oscillator-based embedded clock, given as follows:

$$P_0[n] = t[n] - \sum_{h=1}^{k} \varphi_0 \tag{2}$$

where $t[n] = n\tau_0$ is referred to as the reference time at the nth clock event. In this article, φ_0 equals time synchronization cycle T. Since $\varphi_0 \gg \tau_0$, we assume that the clock updates m_0 times during a single cycle (i.e., $T = m_0\tau_0$). k is calculated from the floor function of n/m_0. That is, $k = \lfloor n/m_0 \rfloor$. The ideal clock resets every m_0 update cycles, let n represent the clock is reset at nth cycle, where $n = \{m_0, 2m_0, 3m_0, \ldots, km_0\}$.

In practice, as a result of the manufacturing tolerance and operating temperatures, $P_i[n]$ of the ith regular node cannot be equal to $P_0[n]$. Based on [16], $P_i[n]$ is given by

$$P_i[n] = t[n] + \frac{\sum_{h=0}^{n-1} \chi_i[h]\tau_0}{f_0} + \frac{\phi_i[n]}{2\pi f_0} - \sum_{h=1}^{k} \varphi_0 \tag{3}$$

where $\chi_i[n] = f_i[n] - f_0$ is the deviation of $f_i[n]$ from f_0, whose accumulated impacts over time are phase fluctuations $\left(\sum_{h=0}^{n-1} \chi_i[h]\tau_0\right)/f_0$. $\phi_i[n]$ represents all the instant phase fluctuations from $t[0]$ to $t[n]$ [31]. Likewise, m_i denotes the number of times for clock updating during T. For the ith clock, it is reset at nth cycle, where $n = \{m_i, 2m_i, 3m_i, \ldots, km_i\}$.

Let the clock offset $\theta_i[n]$ denote the difference between $P_i[n]$ and $P_0[n]$ (i.e., $\theta_i[n] \triangleq P_i[n] - P_0[n]$). The clock skew $\gamma_i[n] \triangleq \chi_i[n]/f_0$ is the normalized difference between $f_i[n]$ and f_0. For theoretical study, we need to modify the one-step update model (2) to a m_i-step update model. By expanding dimension [25] and assuming the auxiliary variable $m_i = m_0$, the drifting clock (2) at the kth synchronization cycle is rewritten as

$$\begin{cases} \theta_i[k+1] = \theta_i[k] + \gamma_i[k]T + \omega_{\theta_i}[k] \\ \gamma_i[k+1] = \gamma_i[k] + \omega_{\gamma_i}[k] \end{cases} \tag{4}$$

where $\omega_{\theta_i}[k]$ and $\omega_{\gamma_i}[k]$ are the Gaussian random noise processes, and the corresponding standard deviations are σ_{θ_i} and σ_{γ_i} [31]. By letting $x_i[k] = [\theta_i[k], \gamma_i[k]]^T$ and $\omega_i[k] = [\omega_{\theta_i}[k], \omega_{\gamma_i}[k]]^T$, the matrix-vector form of (4) is obtained

$$x_i[k+1] = Ax_i[k] + \omega_i[k] \tag{5}$$

where the matrix A is equal to $A = \begin{bmatrix} 1 & T \\ 0 & 1 \end{bmatrix}$. Based on (5), at the kth synchronization cycle, the jitter of the ith clock [in (1)] is expressed as

$$o_i[k] = C_1 x_i[k] \tag{6}$$

where $o_i[k] = \theta_i[k]$ also is known as the controlled output [see (16)]. $C_1 = \begin{bmatrix} 1 & 0 \end{bmatrix}$.

By defining $\mathcal{X}[k] = [x_0^T[k], x_1^T[k], \ldots, x_N^T[k]]^T$ and $\mathcal{O}[k] = [o_0[k], o_1[k], \ldots, o_N[k]]^T$, we extend (6) to the following equation:

$$\mathcal{O}[k] = (\mathcal{I} \otimes C_1)\mathcal{X}[k] \tag{7}$$

where $\otimes$ is the Kronecker product. $\mathcal{I}$ is the $(N+1) \times (N+1)$ identity matrix. In order to obtain good-quality sampled HD-sEMG signals with high SNR, according to (1), we need to keep $\mathcal{O}[k]$ as small as possible. The H_∞ control can be adopted to reduce the jitters $\mathcal{O}[k]$ subjected to drifting clock frequency and varying delays. Hence, in Section IV, we use (5) and (7) to construct a closed-loop BSN synchronization system for H_∞ design, thereby guaranteeing that the sampling jitters are bounded, and also letting the sampling errors be limited.

III. Dynamic Packet-Coupled Synchronization Method

In contrast with the existing works, during each synchronization cycle T, the D-PkCOs protocol transmits a single Sync packet at the allocated time slot [25]. Also, only one timestamp is generated, upon the reception of a Sync packet at the receiver.[3] This Sync packet itself contains the timing information; and it implies that counter of the transmitter matches the threshold value. For example, once $P_0[k]$ of the root node reaches φ_0 at t_k, a Sync packet is immediately sent to the wireless channel. After the packet exchange delay $\kappa[k]$, the ith node produces a timestamp $\hat{P}_i[k]$ by reading the counter register, when it receives Sync. Due to the existence of processing delay $\eta_i[k]$, the correction input (calculated at the time $t_k + \kappa[k]$) is employed to the local clock at $t_k + \kappa[k] + \eta_i[k]$. We also assume that both the packet exchange and processing delays follow the Gaussian distribution.

Once the timestamp $\hat{P}_i[k]$ is obtained, node i computes the offset estimate $\hat{\theta}_i[k]$, in respect of the root node, given as follows:

$$\hat{\theta}_i[k] = \begin{cases} \hat{P}_i[k] - \bar{\kappa} & \text{if } \hat{P}_i[k] - \bar{\kappa} < \frac{\varphi_i[k]}{2} \\ \hat{P}_i[k] - \bar{\kappa} - \varphi_i & \text{if } \hat{P}_i[k] - \bar{\kappa} \geq \frac{\varphi_i[k]}{2} \end{cases} \tag{8}$$

[3]Here, we assume that all the Sync packets from the root node can be successfully received by sensor nodes.

where $\bar{\kappa}$ is the average value of $\kappa[k]$. The D-PkCOs protocol uses the one-way packet exchange strategy for measuring the clock offset. The local timestamp generated on the sensor node contains the packet exchange delay. In the body sensor network, a time slot is allocated to the root node for sending the Sync packet, and there is no need to check whether a wireless channel is busy before the Sync transmission. This means that the Sync packet is directly sent to the channel, and the packet exchange delay $\kappa[k]$ is almost deterministic with little variance [24]. Thus, we can subtract $\bar{\kappa}$ from the timestamp to obtain a more accurate offset estimate.

The clock skew estimate should be calculated from $\hat{\gamma}_i[k] = (\hat{\theta}_i[k] - \hat{\theta}_i[k-1]^+)/T$, where $\hat{\theta}_i[k-1]^+$ is the offset estimate after it is corrected at the $(k-1)$th synchronization cycle. In practice, the value of $\hat{\theta}_i[k-1]^+$ is unknown; however, the offset is close to zero at steady synchronized state. Then, it is reasonable to assume that the clock offset is perfectly adjusted, and $\hat{\theta}_i[k-1]^+$ is zero [16]. Hence, the skew estimate $\hat{\gamma}_i[k]$ can be calculated from the following expression:

$$\hat{\gamma}_i[k] = \frac{\hat{\theta}_i[k]}{T}. \tag{9}$$

Due to the difficulty of real-time counter register access and real-time computation, there always exists a varying processing delay between the reception of a Sync packet and the employment of clock correction input [24]. The use of a feedforward compensation strategy (e.g., [16] and [32]) cannot fully compensate for the effects of this varying delay. Thus, this work utilizes a dynamic controller for clock offset correction, yielding

$$\begin{cases} w_{\theta_i}[k+1] = K_1^{\theta} w_{\theta_i}[k] + K_2^{\theta} \sum_{j=0}^{N} l_{ij}\big(-\hat{\theta}_j[k]\big) \\ \tilde{u}_{\theta_i}[k] = K_3^{\theta} w_{\theta_i}[k] + K_4^{\theta} \sum_{j=0}^{N} l_{ij}\big(-\hat{\theta}_j[k]\big) \end{cases} \tag{10}$$

where $\tilde{u}_{\theta_i}[k]$ is the clock offset correction input. $w_{\theta_i}[k]$ is the offset correction integral controller. K_1^{θ}, K_2^{θ}, K_3^{θ}, and K_4^{θ} are parameters of the dynamic controller for clock offset correction. Also, it can be seen that the PI controller [24] is a particular case of the dynamic controller when setting $K_1^{\theta} = 1$ and $K_3^{\theta} = 1$.

In order to further improve synchronization performance (i.e., reducing the sampling jitters), we also adopt the other dynamic controller for estimating a more accurate skew correction input $\tilde{u}_{\gamma_i}[k]$

$$\begin{cases} w_{\gamma_i}[k+1] = K_1^{\gamma} w_{\gamma_i}[k] + K_2^{\gamma} \sum_{j=0}^{N} l_{ij}(-\hat{\gamma}_j[k]) \\ \tilde{u}_{\gamma_i}[k] = K_3^{\gamma} w_{\gamma_i}[k] + K_4^{\gamma} \sum_{j=0}^{N} l_{ij}(-\hat{\gamma}_j[k]) \end{cases} \tag{11}$$

where $w_{\gamma_i}[k]$ is the integral controller for skew adjustment. K_1^{γ}, K_2^{γ}, K_3^{γ}, and K_4^{γ} are parameters of the dynamic controller for clock skew correction. The moving average method in [21] also is a simplified version of the dynamic controller by letting $K_4^{\gamma} = 0$. Since $w_{\theta_i}[k]$ and $w_{\gamma_i}[k]$ contain the historic (clock offset and skew) information, there is no need to store a number of timestamps. Thus, the dynamic controller reduces computational and memory overheads, compared with maximum likelihood estimation [19] and least squares regression [20].

In consequence of the existence of $\eta_i[k]$, the offset correction input $\tilde{u}_{\theta_i}[k]$ is applied the local sampling clock at $t_k + \kappa[k] + \eta_i[k]$, and this progress can be described as

$$\begin{cases} \theta_i[k]^+ = \theta_i[k]^- + (\tilde{u}_{\theta_i}[k] - (\eta_i[k] + \delta_{\eta_i}[k])) \\ \gamma_i[k]^+ = \gamma_i[k]^- + \tilde{u}_{\gamma_i}[k] \end{cases} \tag{12}$$

where $\theta_i[k]^+/\theta_i[k]^-$ is the clock offset after/before it is corrected at the kth synchronization cycle. $\gamma_i[k]^+/\gamma_i[k]^-$ is the clock skew after/before the drifting clock is adjusted. The value $\delta_{\eta_i}[k]$ is jointly dependent on the skew $\gamma_i[k]$ and the length of the processing delay $\eta_i[k]$ [24]. Note that, instead of only using a PI controller for clock offset correction [24] (or adopting moving average for skew adjustment [21]), this work utilizes the dynamic controller for correcting both the clock offset and skew.

IV. Dynamic Controller Optimization

To guarantee that the sampling jitters are bounded, we use the H_∞ control design to choose eight parameters [see (10) and (11)]. This section starts by constructing a dynamic closed-loop synchronization system. Then, the H_∞ control method is adopted to select a set of parameters in D-PkCOs, thereby guaranteeing that the ratio between the modulus of the sampling jitters and the magnitude of the noises is always less than a given value. This ensures us that we can sample the HD-sEMG signal with a high SNR value.

A. Feedback Control Synchronization System

By defining the measured output $y_i[k] = [\hat{\theta}_i[k], \hat{\gamma}_i[k]]^T$, the measurement equations (8) and (9) are modified to

$$y_i[k] = C_2 x_i[k] + \nu_i[k] \tag{13}$$

where $\nu_i[k] = [\nu_{\theta_i}[k], \nu_{\gamma_i}[k]]^T$ is the estimate noise. $\nu_{\theta_i}[k] = \kappa[k] + \delta_\kappa[k] - \bar{\kappa}$ is the offset estimate noise, and $\nu_{\gamma_i}[k] = (\kappa[k] + \delta_\kappa[k] - \bar{\kappa})/T$ is the skew estimate noise. $\delta_\kappa[k]$ is the extra offset value, which is the joint impacts of skew and the length of corresponding delays [24]. C_2 is the 2×2 identity matrix.

Likewise, let $w_i[k] = [w_{\theta_i}[k], w_{\gamma_i}[k]]^T$ and $u_i[k] = [\tilde{u}_{\theta_i}[k], \tilde{u}_{\gamma_i}[k]]^T$, (10) and (11) can be rewritten as the following form:

$$\begin{cases} w_i[k+1] = K_1 w_i[k] + K_2 \sum_{j=0}^{N} l_{ij}(-y_j[k]) \\ u_i[k] = K_3 w_i[k] + K_4 \sum_{j=0}^{N} l_{ij}(-y_j[k]) \end{cases} \tag{14}$$

where the matrices K_1, K_2, K_3, and K_4, respectively, equal

$$K_1 = \begin{bmatrix} K_1^{\theta} & 0 \\ 0 & K_1^{\gamma} \end{bmatrix}, \; K_2 = \begin{bmatrix} K_2^{\theta} & 0 \\ 0 & K_2^{\gamma} \end{bmatrix}$$

$$K_3 = \begin{bmatrix} K_3^{\theta} & 0 \\ 0 & K_3^{\gamma} \end{bmatrix}, \; K_4 = \begin{bmatrix} K_4^{\theta} & 0 \\ 0 & K_4^{\gamma} \end{bmatrix}.$$

By applying the dynamic correction input $u_i[k]$ to the drifting clock, (5) is modified to

$$x_i[k+1] = Ax_i[k] + Bu_i[k] + \omega_i[k] \tag{15}$$

where B is a 2×2 identity matrix.

Eventually, by including (6), the dynamic output feedback control synchronization system is

$$\begin{cases} x_i[k+1] = Ax_i[k] + Bu_i[k] + Ed_i[k] \\ o_i[k] = C_1 x_i[k] + Fd_i[k] \\ y_i[k] = C_2 x_i[k] + Hd_i[k] \end{cases} \tag{16}$$

with the controller (14), where $o_i[k] = \theta_i[k]$ is the controlled output [also the sampling jitter, as shown in (6)]. $d_i[k] = [\omega_i^T[k], \nu_i^T[k], \eta_i[k] + \delta_{\eta_i}[k]]^T$ is the disturbance. The matrices E, F, and H are, respectively, equal to

$$E = \begin{bmatrix} 1 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix}$$

$$F = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \; H = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix}.$$

Similar to (7), let $\mathcal{U}[k] = [u_0^T[k], u_1^T[k], \ldots, u_N^T[k]]^T$, $\mathcal{D}[k] = [d_0^T[k], d_1^T[k], \ldots, d_N^T[k]]^T$, $\mathcal{Y}[k] = [y_0^T[k], y_1^T[k], \ldots, y_N^T[k]]^T$, $\mathcal{W}[k] = [w_0^T[k], w_1^T[k], \ldots, w_N^T[k]]^T$, a networked closed-loop synchronization system is obtained

$$\begin{cases} \mathcal{X}[k+1] = (\mathcal{I} \otimes A)\mathcal{X}[k] + (\mathcal{I} \otimes B)\mathcal{U}[k] + (\mathcal{I} \otimes E)\mathcal{D}[k] \\ \mathcal{O}[k] = (\mathcal{I} \otimes C_1)\mathcal{X}[k] + (\mathcal{I} \otimes F)\mathcal{D}[k] \\ \mathcal{Y}[k] = (\mathcal{I} \otimes C_2)\mathcal{X}[k] + (\mathcal{I} \otimes H)\mathcal{D}[k] \\ \mathcal{W}[k+1] = (\mathcal{I} \otimes K_1)\mathcal{W}[k] + (\mathcal{I} \otimes K_2)\mathcal{L}(-\mathcal{Y}[k]) \\ \mathcal{U}[k] = (\mathcal{I} \otimes K_3)\mathcal{W}[k] + (\mathcal{I} \otimes K_4)\mathcal{L}(-\mathcal{Y}[k]) \end{cases} \tag{17}$$

where $\mathcal{O}[k]$ represents the sampling jitters, as shown in (7). Note that we can easily verify the pairwise system (16) is controllable. The body sensor network used in this article is a single-hop single-cluster topology. This means that all the pairwise systems are parallel and uncoupled. Hence, the networked system (17) also is controllable.

For simplifying analysis of the system (17), by letting $\bar{x}_i[k] = x_i[k] - x_0[k]$, $\bar{u}_i[k] = u_i[k] - u_0[k]$, $\bar{d}_i[k] = d_i[k] - d_0[k]$, $\bar{o}_i[k] = o_i[k] - o_0[k]$, $\bar{y}_i[k] = y_i[k] - y_0[k]$, and $\bar{w}_i[k] = w_i[k] - w_0[k]$ [25], a reduced networked system is given as follows:

$$\begin{cases} \bar{\mathcal{X}}[k+1] = (\bar{\mathcal{I}} \otimes A)\,\bar{\mathcal{X}}[k] + (\bar{\mathcal{I}} \otimes B)\,\bar{\mathcal{U}}[k] + (\bar{\mathcal{I}} \otimes E)\,\bar{\mathcal{D}}[k] \\ \bar{\mathcal{O}}[k] = (\bar{\mathcal{I}} \otimes C_1)\,\bar{\mathcal{X}}[k] + (\bar{\mathcal{I}} \otimes F)\,\bar{\mathcal{D}}[k] \\ \bar{\mathcal{Y}}[k] = (\bar{\mathcal{I}} \otimes C_2)\,\bar{\mathcal{X}}[k] + (\bar{\mathcal{I}} \otimes H)\,\bar{\mathcal{D}}[k] \\ \bar{\mathcal{W}}[k+1] = (\bar{\mathcal{I}} \otimes K_1)\,\bar{\mathcal{W}}[k] + (\bar{\mathcal{I}} \otimes K_2)\,\bar{\mathcal{L}}(-\bar{\mathcal{Y}}[k]) \\ \bar{\mathcal{U}}[k] = (\bar{\mathcal{I}} \otimes K_3)\,\bar{\mathcal{W}}[k] + (\bar{\mathcal{I}} \otimes K_4)\,\bar{\mathcal{L}}(-\bar{\mathcal{Y}}[k]) \end{cases} \tag{18}$$

where $\bar{\mathcal{X}}[k] = [\bar{x}_1^T[k], \bar{x}_2^T[k], \ldots, \bar{x}_N^T[k]]^T$, $\bar{\mathcal{U}}[k] = [\bar{u}_1^T[k], \bar{u}_2^T[k], \ldots, \bar{u}_N^T[k]]^T$, $\bar{\mathcal{D}} = [\bar{d}_1^T[k], \bar{d}_2^T[k], \ldots, \bar{d}_N^T[k]]^T$, $\bar{\mathcal{O}}[k] = [\bar{o}_1[k], \bar{o}_2[k], \ldots, \bar{o}_N[k]]^T$, and $\bar{\mathcal{Y}}[k] = [\bar{y}_1^T[k], \bar{y}_2^T[k], \ldots, \bar{y}_N^T[k]]^T$, $\bar{\mathcal{W}}[k] = [\bar{w}_0^T[k], \bar{w}_1^T[k], \ldots, \bar{w}_N^T[k]]^T$, $\bar{\mathcal{I}}$ is the $N \times N$ identity matrix, and $\bar{\mathcal{L}}$ is equal to

$$\begin{bmatrix} l_{11} - l_{01} & l_{12} - l_{02} & \ldots & l_{1N} - l_{0N} \\ l_{21} - l_{01} & l_{22} - l_{02} & \ldots & l_{2N} - l_{0N} \\ \vdots & \vdots & \ddots & \vdots \\ l_{N1} - l_{01} & l_{N2} - l_{02} & \ldots & l_{NN} - l_{0N} \end{bmatrix}.$$

The objective of the H_∞ control is to guarantee that the drifting clock and varying processing delay possess a tiny impact on the sampling jitters. This means that, by selecting eight parameters of the dynamic controller, the H_∞ design is to keep $\|\bar{\mathcal{O}}\|_2 / \|\bar{\mathcal{D}}\|_2$ as small as possible. In the following, a design condition is proposed to guarantee that the system (18) is robust in the presence of the perturbations $\bar{\mathcal{D}}[k]$.

B. Controller Design

Here, we first define the H_∞ performance. The transfer function $G[z]$ of (18) relating $\bar{\mathcal{D}}[k]$ to $\bar{\mathcal{O}}[k]$ is $G[z] = \left(\bar{\mathcal{I}} \otimes C_1\right)\left(zI - \left(\bar{\mathcal{I}} \otimes A\right)\right)^{-1}\left(\bar{\mathcal{I}} \otimes E\right) + \left(\bar{\mathcal{I}} \otimes F\right)$. The performance H_∞ of (18) is guaranteed, if the infinity norm $\|G[z]\|_\infty$, which is the two-norm ratio between $\bar{\mathcal{O}}[k]$ and $\bar{\mathcal{D}}[k]$, is less than ρ. That is

$$\|G[z]\|_\infty = \frac{\|\bar{\mathcal{O}}\|_2}{\|\bar{\mathcal{D}}\|_2} < \rho. \tag{19}$$

For theoretical study, and the reduced networked system (18) is modified to the following expression:

$$\begin{bmatrix} \bar{\mathcal{X}}[k+1] \\ \bar{\mathcal{W}}[k+1] \\ \bar{\mathcal{O}}[k] \end{bmatrix} = (\mathbf{A} + \mathbf{BKC}) \begin{bmatrix} \bar{\mathcal{X}}[k] \\ \bar{\mathcal{W}}[k] \\ \bar{\mathcal{D}}[k] \end{bmatrix} \tag{20}$$

where the matrices $\mathbf{A}$, $\mathbf{B}$, $\mathbf{K}$, and $\mathbf{C}$ are, respectively, equal to

$$\mathbf{A} = \begin{bmatrix} \bar{\mathcal{I}} \otimes A & 0 & \bar{\mathcal{I}} \otimes E \\ 0 & 0 & 0 \\ \bar{\mathcal{I}} \otimes C_1 & 0 & \bar{\mathcal{I}} \otimes F \end{bmatrix}, \; \mathbf{B} = \begin{bmatrix} 0 & \bar{\mathcal{I}} \otimes B \\ I & 0 \\ 0 & 0 \end{bmatrix}$$

$$\mathbf{K} = \begin{bmatrix} \bar{\mathcal{I}} \otimes K_1 & -(\bar{\mathcal{L}} \otimes K_2) \\ \bar{\mathcal{I}} \otimes K_3 & -(\bar{\mathcal{L}} \otimes K_4) \end{bmatrix}, \; \mathbf{C} = \begin{bmatrix} 0 & I & 0 \\ \bar{\mathcal{I}} \otimes C_2 & 0 & \bar{\mathcal{I}} \otimes H \end{bmatrix}.$$

Lemma 1 ([16], [33]): Given the square matrices X and S, and the matrices $\mathsf{T} = \mathsf{T}^T$, A, P, L with the appropriate dimensions, the following two inequalities are equivalent:

$$\begin{bmatrix} \mathsf{T} + (\mathsf{LA}) + (\mathsf{LA})^T & * \\ \mathsf{XP}^T - \mathsf{XL}^T + \mathsf{SA} & -\mathsf{SX}^T - \mathsf{XS}^T \end{bmatrix} < 0 \tag{21}$$

$$\mathsf{T} + (\mathsf{PA}) + (\mathsf{PA})^T < 0. \tag{22}$$

Theorem 1: Consider a directed single-hop single-cluster body sensor network represented by $\mathcal{G}$, consisting of an ideal root node's clock and N leaf node clocks with the drifting frequencies $f_i[k] \in \{f_i[k] : f_i[k] \neq f_0 \text{ and } i \in \mathcal{N}\}$, and a scalar $\rho > 0$. For the known parameters ζ and $\xi \neq 0$, if there exist the matrices $Q > 0 \in \mathbb{R}^{4N \times 4N}$, $G \in \mathbb{R}^{5N \times 5N}$, $V \in \mathbb{R}^{4N \times 4N}$, and

$U \in \mathbb{R}^{4N\times 4N}$ such that

$$\begin{bmatrix} \Gamma & * & * \\ \Lambda & \Omega & * \\ \Phi & \Psi & \Upsilon \end{bmatrix} < 0 \tag{23}$$

where $\Gamma = -\text{diag}(Q, \rho^2 I) + (\zeta H\mathbf{B}V\mathbf{C}) + (\zeta H\mathbf{B}V\mathbf{C})^T$, $\Lambda = G\mathbf{A} + \mathbf{B}V\mathbf{C}$, $\Omega = -G - G^T + \text{diag}(Q, I)$, $\Phi = (\mathbf{B}^T\mathbf{B}V\mathbf{C}) - (\zeta H\mathbf{B}U)^T$, $\Psi = (\xi G\mathbf{B} - \mathbf{B}U)^T$, $\Upsilon = -(\mathbf{B}^T\mathbf{B}U) - (\mathbf{B}^T\mathbf{B}U)^T$, $H = I \in \mathbb{R}^{5N\times 5N}$, and the gain matrix is obtained from $\mathbf{K} = \xi U^{-1}V$, then the performance H_∞ of $\mathcal{G}$ is guaranteed.

Proof: Suppose that (23) holds, $\Upsilon < 0$ indicates that U is a nonsingular matrix. Let $U = \xi\mathbf{U}$, and compare (21) with (23), we have

$$\mathsf{T} = \begin{bmatrix} -\text{diag}(Q, \rho^2 I) & * \\ \Lambda & \Omega \end{bmatrix}$$

$$\mathsf{P} = \begin{bmatrix} 0 & \Psi \end{bmatrix}^T,\ \mathsf{S} = \mathbf{B}^T\mathbf{B}\mathbf{U},\ \mathsf{X} = \xi I$$

$$\mathsf{L} = \begin{bmatrix} (\zeta H\mathbf{B}\mathbf{U})^T & 0 \end{bmatrix}^T,\ \mathsf{A} = \mathbf{U}^{-1}V \begin{bmatrix} \mathbf{C} & 0 \end{bmatrix}.$$

In Lemma 1, as a result of the equivalence relation between (21) and (22), the following inequality is given:

$$\begin{aligned} &\begin{bmatrix} -\text{diag}(Q, \rho^2 I) & * \\ \Lambda & \Omega \end{bmatrix} \\ &\quad + \left(\begin{bmatrix} 0 & I \end{bmatrix}^T (G\mathbf{B} - \mathbf{B}\mathbf{U})\, \mathbf{U}^{-1}V \begin{bmatrix} \mathbf{C} & 0 \end{bmatrix} \right) \\ &\quad + \left(\begin{bmatrix} 0 & I \end{bmatrix}^T (G\mathbf{B} - \mathbf{B}\mathbf{U})\, \mathbf{U}^{-1}V \begin{bmatrix} \mathbf{C} & 0 \end{bmatrix} \right)^T \\ &= \begin{bmatrix} -\text{diag}(Q, \rho^2 I) & * \\ \Lambda + (G\mathbf{B} - \mathbf{B}\mathbf{U})\, \mathbf{U}^{-1}V\mathbf{C} & \Omega \end{bmatrix} < 0. \end{aligned} \tag{24}$$

Let $\mathbf{K} = \mathbf{U}^{-1}V$, (24) is modified to

$$\begin{bmatrix} -\text{diag}(Q, \rho^2 I) & * \\ G\mathbf{A} + G\mathbf{B}\mathbf{K}\mathbf{C} & -G - G^T + \text{diag}(Q, I) \end{bmatrix} < 0. \tag{25}$$

Based on [34], (25) is the bounded real lemma with the auxiliary variable matrix G. Once the matrix inequality (23) is established, the H_∞ performance ρ of the reduced system (20) is guaranteed. ■

Theorem 1 implies that, under the design condition of the linear matrix inequality (23), the body sensor network $\mathcal{G}$ possesses the H_∞ performance. This means that the two-norm ratio between $\bar{\mathcal{O}}[k]$ and $\bar{\mathcal{D}}[k]$ is less than ρ. In the directed single-hop single-cluster BSN, the perturbations $\mathcal{D}[k]$ (from the drifting clock and delays) have a tiny impact on the sampling jitters, and all the BSN nodes' sampling errors are bounded. Also, based on (1), the body sensor network can sample the HD-sEMG signal with a high SNR value.

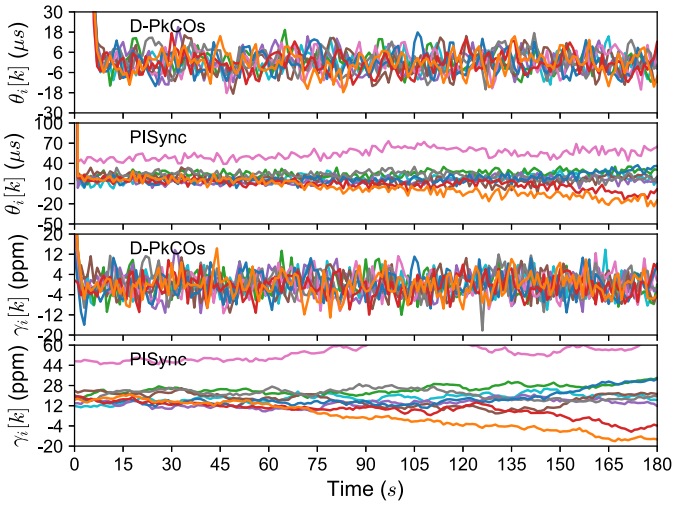

Fig. 2. Evolution of the clock offset $\theta_i[k]$ and skew $\gamma_i[k]$ under the D-PkCOs and PISync synchronization protocols.

V. Evaluation of D-PkCOs

In this section, we start with a performance investigation of the D-PkCOs protocol via numerical simulations. Then, D-PkCOs is implemented on a hardware testbed, and is also studied in a 10-node body sensor network. Moreover, several synchronization protocols (e.g., PISync) are selected for comparison.

A. Simulation Results

We conduct simulations in a directed 10-node BSN. The initial offset $\theta_i[0]$ and $\gamma_i[0]$ are randomly configured following the uniform distribution in the corresponding intervals (400 and 0.8 ms) and (0 and 50 ppm). Meanwhile, the clock offset and skew are, respectively, subject to random perturbations with the standard deviations $\sigma_{\theta_i} = 1$ μs and $\sigma_{\gamma_i} = 1$ ppm. The packet exchange delay's standard deviation is 4 μs [24]. The synchronization cycle is 1 s. From Theorem 1, the H_∞ performance $\rho = 5.24$, and four matrices K_1, K_2, K_3, and K_4 of the dynamic controller are obtained under $\zeta = 0.254$ and $\xi = 0.385$:

$$K_1 = \begin{bmatrix} 0.0519 & 0 \\ 0 & 0.0519 \end{bmatrix}$$

$$K_2 = \begin{bmatrix} -0.000000000000245 & 0 \\ 0 & 0.0000000000000149 \end{bmatrix}$$

$$K_3 = \begin{bmatrix} 0.0000227 & 0 \\ 0 & 0.00000591 \end{bmatrix},\ K_4 = \begin{bmatrix} 0.804 & 0 \\ 0 & 0.761 \end{bmatrix}.$$

Fig. 2 shows the evolution of offset and skew in the simulations. Both D-PkCOs and PISync let the offset and skew approach to zero, and thus, the network realizes steady synchronized state. The PISync protocol utilizes the full offset estimate to adjust the drifting clock (i.e., $K_1^\theta = K_2^\theta = K_3^\theta = 0$

TABLE I
PARAMETER SETTINGS OF PISYNC, DCBTS, AND TPSN[4]

	PISync	DCBTS	TPSN
K_1^θ	0	0	0
K_2^θ	0	0	0
K_3^θ	0	0	0
K_4^θ	1	0.5	1
K_1^γ	0	0.5	0
K_2^γ	0	0.5	0
K_3^γ	0	0.5	0
K_4^γ	3.05×10^{-8}	0	1

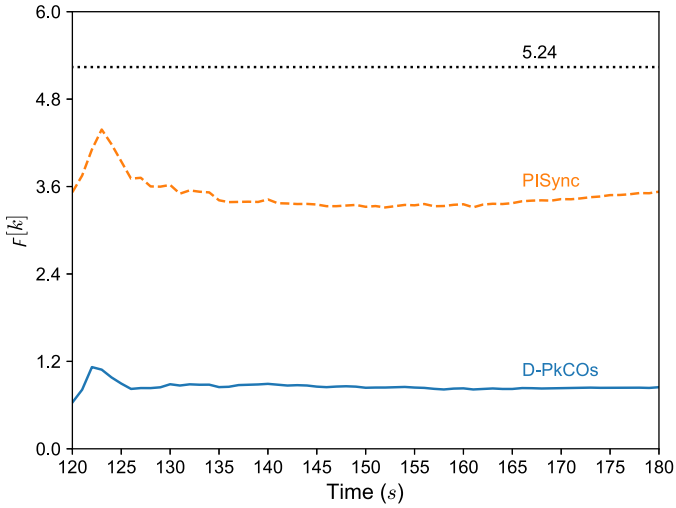

Fig. 3. Evolution of $\mathcal{F}[k] = \sqrt{\sum_{h=0}^{k} \mathcal{O}^T[h]\mathcal{O}[h] / \sum_{h=0}^{k} \mathcal{D}^T[h]\mathcal{D}[h]}$ via the D-PkCOs and PISync protocols.

and $K_4^\theta = 1$, see Table I), its convergence speed is faster than that of D-PkCOs (where $K_4^\theta \approx 0.804$).

In PISync, a P controller also is used for clock skew correction (where $K_1^\gamma = K_2^\gamma = K_3^\gamma = 0$, as given in Table I). Even though the adaptive tuning solution is adopted, the little value of K_4^γ (in the P controller) still cannot overcome the impacts of the drifting clock frequency (see Fig. 2). The P controller is a simplified version of the dynamic controller; by using the dynamic controller's parameters obtained from Theorem 1, the adjusted skew under D-PkCOs is much smaller at steady state. Moreover, our protocol also adopts the dynamic controller to correct clock offset, while only the P controller is used in PISync for offset adjustment. Thus, with the aid of the proposed Theorem 1, the D-PkCOs algorithm can achieve better performance, compared with the PISync method (see Fig. 2).

From Fig. 3, the behavior of the steady-state offset is also reflected in the evolution of $\mathcal{F}[k]$[5]. Even though both D-PkCOs and PISync guarantee that $\mathcal{F}[k]$ of the BSN is less than $\rho = 5.24$,

[4]In PISync, $K_4^\gamma = 3.05 \times 10^{-8}$ is the maximum value, it varies according to the adaptive parameter tuning method in [26].

[5]$\mathcal{F}[k]$ represents the value of $\|\bar{\mathcal{O}}\|_2/\|\bar{\mathcal{D}}\|_2$ at the kth synchronization cycle [see (19)].

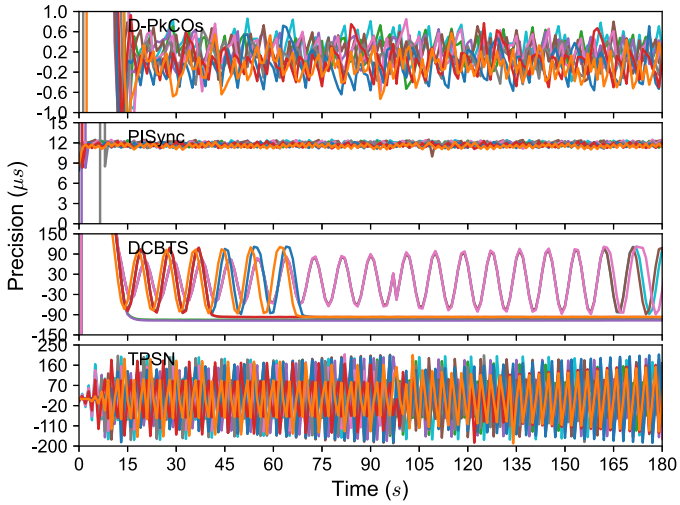

Fig. 4. Evolution of the synchronization precision via four protocols.

$\mathcal{F}[k]$ in D-PkCOs is only around one third of $\mathcal{F}[k]$ in PISync at steady synchronized state.

B. Experimental Evaluation

In addition to the simulations, we also study the performance of the D-PkCOs synchronization protocol in the same 10-node BSN. For the implementation, $P_i[n]$ is represented by a 32-bit counter register of the clock module on the Atmel SAM R21 board [35], which adopts an external 32.768 MHz crystal oscillator as the clock source. The threshold register is 32 767 999 to let the clock reset each second. Once the counter value matches threshold, the processor triggers a hardware interrupt, where counter is reset to zero, meanwhile, a Sync packet is transmitted for synchronization purposes. On the reception of the Sync packet, the other hardware (address match) interrupt is issued to generate a local timestamp, which is utilized for offset estimation and clock correction. Note that, due to the difficulty of adjusting clock frequency in an embedded system, the threshold correction method is considered as a substitute solution [16].

During the experiments, the GPS-disciplined clock [36] is connected to the root node ($i = 0$), for providing the reference time to the wireless network. The synchronization cycle T is 1 s. The mean value of the packet exchange delay is about 514.25 μs, and its standard deviation is of 0.3 μs. The dynamic controller gain is set to the same parameters used in the simulations. The logic analyzer [37] is used to evaluate performance, and the precision is defined as the time difference between the ith leaf node clock and root node's clock. We select three protocols (i.e., PISync, DCBTS, and TPSN) for comparison, and their configurations are presented in Table I.

Both PISync and TPSN adopt the P controller structure for offset and skew correction, the use of the adaptive K_4^γ tuning solution in PISync can let the network achieve better synchronization precision (i.e., the sampling jitters) of around 13 μs (see Fig. 4). Even though DCBTS utilizes the moving average method (with the same parameter settings in [21]) for clock skew

TABLE II
SYNCHRONIZATION PERFORMANCE OF FOUR ALGORITHMS

	D-PkCOs	PISync	DCBTS	TPSN
Mean (μs)	0.117	11.783	100.322	8.161
Std dev (μs)	0.277	0.333	4.299	104.883

correction, only the performance of about 110 μs is obtained in the network, which is worse than the reported performance in [21]. This may be due to the inappropriate parameter selection, and more careful parameter configuration is needed for different hardware platforms. From Fig. 4, by using the control gain obtained from Theorem 1, the D-PkCOs protocol can realize clock synchronization with the precision of around 1 μs in the body sensor network, which is better than the performance of PISync (around 13 μs), DCBTS (about 110 μs), and TPSN (approximately 210 μs). In addition, the average values and standard deviations of synchronization precision (which also is the sampling jitter) in the 10-node BSN are summarized in Table II. In addition, we find that the processing delay is not a perfect Gaussian noise. Thus, more investigations are needed in the future to have a better understanding of how the performance is affected by the non-Gaussian noise.

VI. APPLICATION OF D-PKCOS IN THE HD-SEMG AUTHENTICATION SYSTEM

In this section, we use the Hyser dataset [9] to study the effectiveness of D-PkCOs in the HD-sEMG-based authentication system (through the hand gesture classification). Four electrode arrays are connected via cables, and are also placed on the forearm's extensor and flexor muscles for collecting the Hyser data, where 20 volunteers (i.e., subjects) participate and perform 34 commonly used hand gestures. This dataset is acquired at the sampling rate of 2048 Hz. The single-hop single-cluster topology is widely used in the BSN; then, we assume that these four electrode arrays construct a wireless network by using this topology (i.e., a single-cluster BSN consisting of one root node and four leaf nodes, see Fig. 1). During the simulations, we resample the Hyser data at 10 240 Hz; in the meantime, the sampling jitters, which are randomly generated according to the mean values and standard deviations of four protocols (see Table II), are introduced.

Fig. 5 presents the original sEMG signal (from Subject 5) in the 1-s sampling duration. The biosignal voltage is between around -300 and $+300$ μV. The evolution of the sampling error in different protocols is also shown in Fig. 5. Clearly, the synchronization performance has a significant effect on the sampled signal quality. The D-PkCOs algorithm guarantees that the sampling error is less than 0.5 μV. However, by using the DCBTS synchronization protocol, the sampling error is about 30 μV. Thus, our D-PkCOs synchronization protocol can let the body sensor network acquire a high-quality signal (with a small sampling error). This also is reflected in the sampled HD-sEMG signal's SNR values (see Fig. 6). For example, the signal's SNR value is around 60 dB under the D-PkCOs protocol; while, by

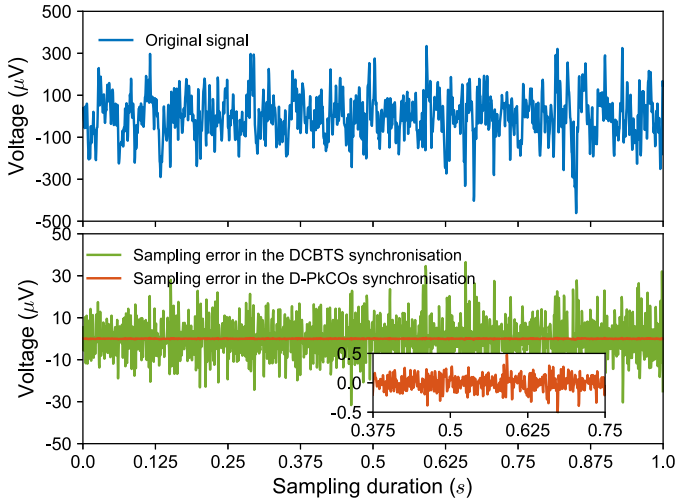

Fig. 5. Original sEMG signal, and sampling error in the D-PkCOs and DCBTS synchronization protocols.

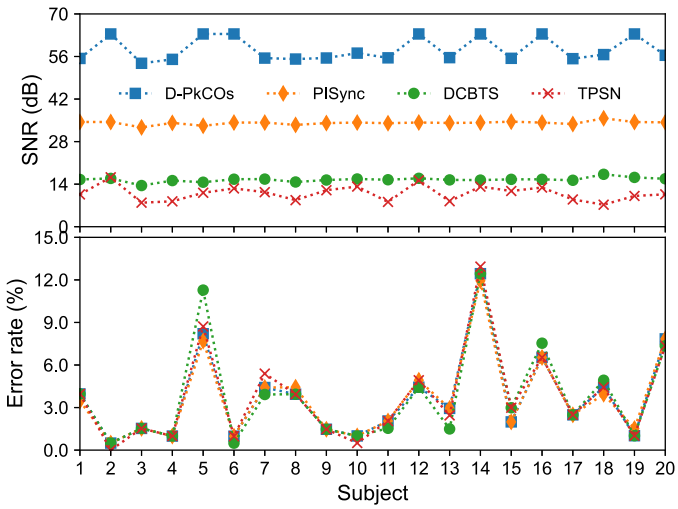

Fig. 6. SNR and maximum classification error rate under four protocols.

utilizing TPSN, the HD-sEMG biosignal with SNR of about 10 dB is acquired.

We use the LDA-based method to classify and recognize 34 hand gestures, and the maximum classification error rate is shown in Fig. 6. Overall, the classification performance under D-PkCOs is slightly better than that of using the other three protocols. However, when it comes to Subject 5, our D-PkCOs protocol can let the authentication system obtain a smaller maximum classification error of 8.205%, compared with 11.282% via DCBTS.

VII. CONCLUSION

In this article, we adopt a D-PkCOs protocol to synchronize data sampling clocks in a body sensor network, thereby realizing simultaneous biosignal acquiring among distributed electrode arrays for biometric authentication. The D-PkCOs protocol only

requires one Sync packet during each synchronization cycle, which reduces the communication overhead. To realize precise sampling of all BSN nodes subject to drifting clock frequency and varying processing delay, we adopt a dynamic controller to adjust both the clock offset and skew for reducing the sampling jitters. This solution possesses the benefits of automatically removing the effects of varying processing delay, and estimating a more accurate clock skew for adjustment. In addition, we also use the H_∞ control method to design parameters of the D-PkCOs synchronization protocol. Thus, in the BSN, the drifting clock and varying processing delay possess a tiny impact on the sampling jitters, and all the nodes' sampling errors are bounded. The experimental results demonstrate that our D-PkCOs protocol can keep the sampling jitters less than 1 μs in a 10-node IEEE 802.15.4 network. The application of D-PkCOs to the BSN shows that the HD-sEMG signal with a high SNR value is obtained, which leads to better gesture classification performance.

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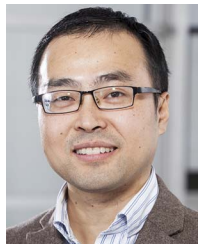

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