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Evolvable Embryonics: 2-in-1 Approach to Self-Healing Systems

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Abstract

This paper covers the authors' recent research in the area of evolutionary design optimisation in electronic application domain (Evolvable Hardware). This will be also presented in the context of biologically inspired systems where Evolvable Hardware is concerned with evolutionary synthesis of self-healing systems and potentially hardware capable of online adaptation to dynamically changing environment. We will also illustrate how EAs can produce novel and unintuitive design solutions, and possibly new design principles. The novelty of this research project addresses this compelling change in the traditional landscape of the associated research disciplines by seeking to provide a novel biologically inspired mechanism to support the design optimisation of self-healing architectures, that is Evolvable-Embryonics.

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1. Introduction

The electronic circuit industry is increasing in complexity very rapidly. With new generations of hardware, the demand for more complex behaviours is, consequently, growing. These circuits are typically designed to either be part of a system, or to be the system itself; computers, digital watches, nuclear power stations, just to mention a few. Without any doubt, these systems perform better than human beings in many aspects. However, despite these achievements, hardware failures to fulfil some real life tasks are common; and even current leading computer systems fall short in performing them, when a changing environment is considered. These failures can be explained by limitations of the traditional circuit design methodologies, which are based on rules that have been expanded over the years and depend only on human capabilities. Discovering how to design a rather undemanding (in terms of silicon or other technology resources) reconfigurable hardware system or circuit, together with fault tolerance capabilities, has been a real challenge to researchers and engineers in the last few decades. Alternative inspirations have been desirable in this context, and a system that can exhibit capabilities of self-reproduction, self-healing and adaptation could represent a ground-breaking advance. These capabilities are more known in biological systems. Steps towards these artificial machines and artificial life, which exhibit attributes such as those found in their biological counterparts, have already taken place in recent technological and research advances. The human nervous and immune systems have inspired research on Artificial Neural Networks (ANN) [1] and Artificial Immune Systems [2], respectively. In addition, in the recent decades scientists started to exploit other complex biological systems and processes such as embryology, and evolution, which, respectively, inspired research on Embryonics [3], and Evolvable Hardware [4,5].

Typically, an Embryonics System is a homogenous array that consists of a number of identical *embryonic* cells. Together, these cells incorporate self-repair and self-healing mechanisms. On one hand, this method, relatively, allows the hardware device to be more reliable, on the other hand, it

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proved to be very inefficient as far as complexity is concerned.

Evolutionary Algorithms (EA) proved, in many cases, to outperform human design and the traditional trial-and-error approaches, which are time consuming and require highly skilled engineers/experts. Unlike the human expert, EA explores a much larger solution space and the probability of making mistakes with conventional approaches is very high (local optima), which would require going through the whole design cycle to rectify. The design optimisation of Complex Systems is often a multidisciplinary task and involves multiple conflicting objectives and design constraints, where conventional methods cannot solve efficiently. The application of EAs in electronic system design signifies Evolvable Hardware (EHW) or Evolutionary Electronics (EE).

In this paper we will cover the authors' recent research in the area of Evolutionary Design Optimisation in Electronics application domain. An illustration of how EAs can produce new design patents and new design principles in both analogue and digital electronics is also presented. A novelty of this research addresses the compelling change in the traditional landscape of the associated research disciplines by seeking to provide a novel biologically inspired mechanism to support the design optimisation of self-healing architectures, namely, Evolvable Embryonics.

2. Evolvable Hardware

EHW refers to reconfigurable electronic systems, which can evolve under the control of some EAs, in order to solve real-world tasks. EHW is a technology that can allow hardware to evolve until an optimal or near-optimal solution to a certain problem or desired behaviour is achieved. This technology was proposed as an alternative to traditional design paradigms. This technique has seen some considerable advances during the past decade. Researchers have approached the field of EHW from two distinct angles which are intimately related [6]. First is the use of EAs for circuit synthesis and design, as an alternative to traditional methods applied in man-made circuitry [7], mostly known as Evolutionary Electronics. As an ultimate goal, the second is the use of EAs to develop a new generation of hardware, self-reconfigurable and evolvable, environment-aware, which can adaptively modify its structure to attain a desired behaviour optimally, mostly known as EHW. As such, it will be able to survive and recover from faults and degradation, and also improve its performance over the lifetime of operation. The latter point is often known as hardware capable of online adaptation to a dynamically changing environment. EHW has been applied on three hierarchical levels, Transistor [8], Gate [9] and Functional [10] levels. Also, EHW can be *Direct* or *Indirect*, according to the level of genotype representation. Moreover, EHW is categorised into *Extrinsic*, *Intrinsic* and *Mixtrinsic* [11]. This classification is based on how solutions are evaluated and tested. This can be offline with a simulator (Extrinsic) or online in the actual hardware (Intrinsic). The third category was proposed to solve the portability problem between the real hardware and the simulator and vice versa.

One important feature of design through evolution is the possibility for discovering novel topologies to a problem solution that may prove difficult to be realised by conventional approaches [12]. For some complex problems, designing these topologies may even be beyond human abilities. Sections 2 and 3 illustrate this feature in two case studies, digital and analogue systems, respectively.

3. Digital Evolutionary Electronics (D-EE)

One of the early works in evolutionary digital electronics was published by Louis [13]. Since then, this field - Evolutionary Electronics - started to receive more attention by an increasing number of researchers. Many aspects have been discussed and many techniques have been developed in EE; however, only handful researchers have investigated one of the EE greatest potentials: design innovation. Research reported in [14-17] has also illustrated the evolutionary design invention on combinational circuits, particularly, arithmetic logic functions. The author(s) of [16] demonstrated how the GA could re-discover the well-known ripple-carry principle for building adder circuits of any size. They also examined some novel designs for binary multipliers of different complexities.

Two real world applications are used in this section as case studies to verify the hypothesis of the evolutionary design innovation. The authors were first to attempt these case studies which are reported by the authors in greater details in [12] and [18], therefore, only the main highlights are presented herein in order to serve the context of this paper. For more specific details, readers are referred to [12] and [18]

3.1. Case Study 1

In this case study a design by evolution in illustrated by a Seven-Segment Decoder; a real-world application that is embedded, in almost all numeric digital devices. The EA employed has successfully generated a circuit topology for the seven segment decoder Figure 1. This solution, compared to a human most efficient design using Karnaugh Map (designed by the authors), illustrated in Table 1, is far more efficient, with only 18 2-input gates against 32. This is a significant improvement approximating to 80%.

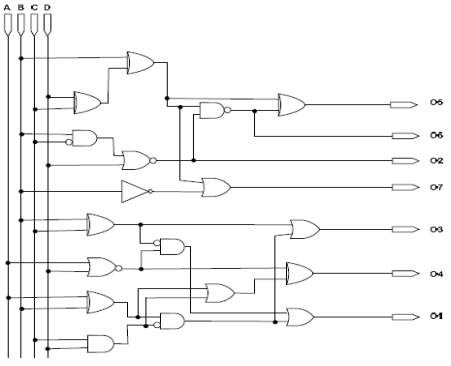

Fig. 1. Evolved BCD-to-Seven- Segment Decoder logic diagram

Table 1 BCD-to-Seven- Segment Decoder logic produced by Karnaugh Maps

Output1 = A + B D + C + B' D'
Output2 = A + C' D' + CD+ B'
Output3 = A + B + C' + D
Output4 = B' D' + C D' + (B C')D + B' C
Output5 = B' D' + CD
Output6 = A + C' D' + B D' + B C'
Output7 = A + C D' + B C' + B' C
Total Number of 2-input gates = 32

3.2. Case Study 2

A more complex real world application of combinational digital circuitry, a *32-Step Traffic Lights Controller* is presented as a case study, which has never been attempted in the evolutionary electronics literature. This Traffic Light controller is implemented as a combinational logic circuit (decoder) with 5 inputs, indicating time and 6 outputs that indicate Green, Yellow and Red lights of North/South and East/West traffic light. When linked to a counter with a clock, the circuit's inputs cycle continuously, causing the traffic light to cycle through its outputs to generate the traffic signals defined in Table 2.

Table 2 The Traffic Signals sequences Sought

Time range	North-South	East-West
0-7	Green	Red
8-10	Yellow	Red
11-12	Red	Red
13-20	Red	Green
21-23	Red	Yellow
24	Red	Red
25-31	Flashing Red	Flashing Red

Using a Karnaugh Maps for each output line, the Boolean logic expression for each traffic light signal is generated. From Table 3, one can count 50 2-input gates and 11 inverters, however, after removing the obvious gate redundancy, the circuit can be reduced to 39 2-input gates and 11 inverters.

Table 3 Boolean Logic Expressions for the Traffic Lights Outputs using K-Maps

North/South
Green = *(A + B)`*
Yellow = *[(A + B` + C + E)(A + B` + C + D)]`*
Red = *[(A` + B)(A` + E)(A + B` + C`)(A + B` + D` + E`)]`*
East/West
Green = *[(A` + B + C)(A + B` + C` + E`)(A + B` + C `+ D`)(A` + B + C`)(D + E)]`*
Yellow = *[(A` + B + C` + E`)(A` + B + C` + D`)]`*
Red = *[(A + B)(A + C)(A` + B` + E)(B` + C` + D + E)]`*

The employed EA was successful in producing a correct and a more efficient circuit, with only only 18 2-input gates, 2 2:1 MUX and 2 inverters. The schematic representation of this circuit is shown in Figure 2. This problem was not a straightforward task for any automated design tool, especially that it was evolved as a whole with all outputs simultaneously. The EA-produced solution is highly unintuitive with more interdependencies, which is very difficult, if not impossible, to construct using conventional methods.

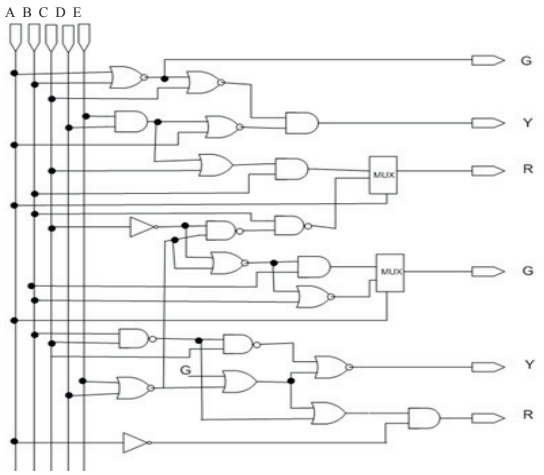

Fig. 2 Schematic representation of a Traffic Light Controller described above, evolving multiple inputs together.

It is interesting to observe the way Evolutionary Algorithms could achieve solutions that may not be obvious to the human designer. It outperformed the traditional paradigms by the efficient reuse of modules within a circuit to reduce the total number of components/gates. Both case study presented are excellent examples where the GA could excel as an alternative design tool for real-world digital industrial applications. Researchers, like Miller, have already discussed the potential to extract some new design rules form these novel designs, produced as a result of an evolutionary process [14-16].

4. Analogue Evolutionary Electronics A-EE)

Figure 3 illustrates of the experiment environment which allows the evolutionary synthesis of analogue electronic circuit designs via extrinsic evolution (off-line). To the best of the authors' knowledge, multi-objective optimization has never been applied before for passive analogue circuits and only in one occasion for active circuits. The implementation of this framework integrates an analogue circuits' simulator, PSpice and a Multiobjective Genetic Algorithm (MOGA-II).

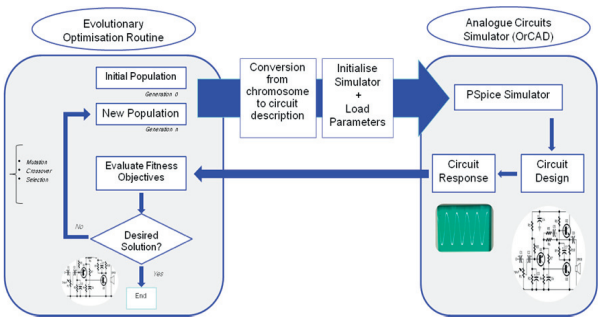

Fig. 3 A-EE Experiment Environment

The design of passive filters, especially, the High Pass Filter is a typical case study experimented with in the A-EE research. A respectable number of researchers in A-EE have concentrated their efforts on the evolution of passive filters; this provides the authors with the opportunity to compare the obtained results using the developed framework with the ones reported in literature. This way the presented approach can be validated and its effectiveness can be measured. The specifications (Table 4) selected for this evolution-based optimization are the ones used in Koza et al. in [19]. The experimental parameter settings are presented in Table 5. The objectives are to obtain the desired frequency response (F1 in *Equation 1*) with the minimum number of components with minimal evaluations. The stopping criteria for each experiment, is either to achieve satisfactory results achieving maximum number of generations.

$$F_1 = \sum_{i=0}^{95} W(d(f_i), f_i) \cdot d(f_i) \quad (1)$$

$$d(f_i) = \left| V_{OUT}(f_i) - V_{TARGET}(f_i) \right| \quad (2)$$

Table 4 High Pass filter specifications

Passband (2kHz-100kHz)	Stopband (0Hz-1000Hz)
$V_{TARGET} = 1$ $W(d(f_i), f_i) = \begin{cases} 0 & if \quad d(f_i) = 0 \\ 1 & if \quad d(f_i) \le 0.03 \\ 10 & if \quad d(f_i) > 0.03 \end{cases}$	$V_{TARGET} = 0$ $W(d(f_i), f_i) = \begin{cases} 0 & if \quad d(f_i) = 0 \\ 1 & if \quad d(f_i) \le 0.001 \\ 10 & if \quad d(f_i) > 0.001 \end{cases}$

Table 5. Experimental parameter settings for MOGA-II

MOGA-II	
Crossover rate	10-80%
Probability of Selection	40-70%
Probability of Mutation	40-80%
Population	50-500
Generations	Up to 5000

Figure 4 depicts an evolve solution of High Pass Filter, which was produced using the presented experiment environment driven by MOGA-II. The solution uncovers a very known human topology solution (*Four-Rung Ladder* high pass filter), also produced by the evolutionary process run by Koza [19], but with much improved frequency response (F1), less components and considerably less evaluations. Table 6 captures important work in the A-EE on High Pass filter reported by prominent authors in the field with the same specifications, and compared with the results illustrated in Figure 4.

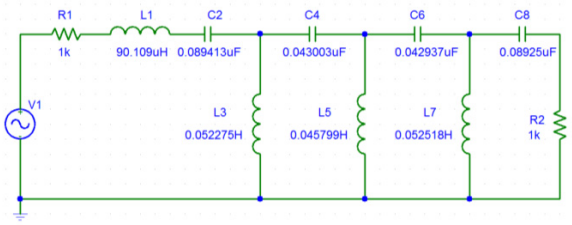

Fig. 4 More competitive High Pass Filter by evolution

Table 6 Comparing the solution depicted in Figure 4

	Ideal Filter	10 order Chevyshev Filter	Koza et al. ladder	Hu et al., 2005	Multiobjective Optimisation Framework
Max. attenuation in pass-band (dB)	0	1.7	1.798	Not Known	1.14
Max. attenuation in stop-band (dB)	-∞	-82	-68	Not Known	-54
Fitness value F_1	0	0.097	0.213	0.32	0.04358
No. Elements	-	10	9	27	8
No. Individuals	-	-	17,280,000	500,000	71,847
Circuit simulator	-	-	MicroSim	MATLAB	OrCAD

This comparative table clearly shows the superiority of the multi-objective evolution in A-EE over single objective. In less than 72,000 function evaluations, a solution of only 8 components with only 0.0436 % error in frequency was uncovered. This is a very competitive solution compared to all solutions reported from literature, either designed by evolution or by human. Considering the significant reduction in computational time required to converge, the case obtained solution, driven by MOGA-II can also be claimed superior.

The voltage and attenuation responses of this evolved circuit are shown in Figure 5 and Figure 6, respectively. The main features of this response are a maximum absolute attenuation of 1.14dB in the pass-band and a maximum attenuation of -54 dB in the stop-band.

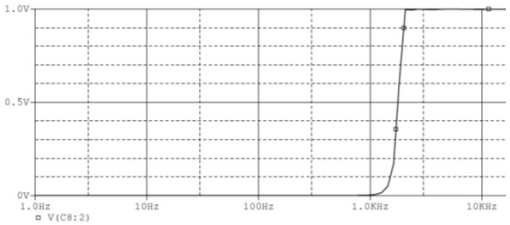

Fig. 5 evolved High Pass Filter: Voltage response

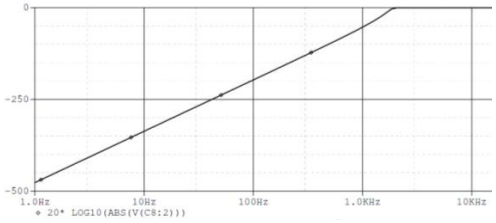

Fig. 6 evolved High Pass Filter: Attenuation response

5. Evolving an Embryonics Systems

In Sections two and three, it has been illustrated that Evolutionary Electronics (EE) can innovatively solve some complex digital and analogue circuit design problems by arriving at unusual designs which efficiently exploit available resources, using offline evolution. This section explores the application of EE in a highly complex biologically inspired fault tolerant system- Embryonics.

Traditionally, there are two main approaches to increasing reliability in systems: fault prevention and fault tolerance. Fault prevention is the prevention of fault occurring in a system; although leading to a set of well-respected design techniques, this method of increasing reliability is inevitably weakened by the fact that it is impossible to eliminate the possibility of a fault. Fault tolerant systems are systems that will continue to operate correctly even in the presence of a fault. Fault tolerance is a useful concept only in improving the reliability of systems that are already highly reliable, because it should be used as a supplement to, and not a replacement for, reliable design and components. Some fault tolerant systems offer what is termed 'graceful degradation'. Graceful degradation is when the system recognises the presence of a fault and reverts to a more basic and reliable mode of operation. This offers an insurance against a more complicated (and therefore inherently more prone to faults) system failure, although the presence of a fault compromises the system's performance, it will maintain essential functionality. The application of EE to evolve this type of fault tolerance systems, namely, circuits with concurrent error detection (CED), or Self-Checking Circuits, was only addressed by [22].

Research in Embryonics is fairly recent. Inspired by biological embryonic development, the idea was developed to emulate this process with the ability to tolerate faults in digital systems. This is an unconventional paradigm for hardware reliability. Embryonics Hardware System satisfies the fundamental characteristics which contribute to the development of any multi-cellular living being. Researchers' attempts on this field have been successful; they proved the feasibility of mimicking nature into the world of digital electronics where self-repair and self-healing mechanisms, found in living beings, are moderately applied successfully. However the human design results in very complex hardware architectures, which stipulates large number or electronic resources. The objective of the work presented in this section is to reconstruct this complex parallel cellular hardware system architecture, the Embryonics, into simpler forms, which comply with equivalent functionalities and performance, by employing the biological principle of natural evolution to artificial systems using techniques of evolutionary computation.

The Embryonic system model adopted in this work follows the same structural hierarchy as that found in [20] and [21] organism structure. The Embryonic system proposed herein adopts the row-elimination process to exhibit fault tolerance Figure 7. In row elimination, when one cell, in the cellular array, is infected it causes the whole corresponding row to become transparent, it is eliminated from functional use. The original row shifts to the north finding a spare row to be substituted. This method is adopted by other researchers in the field [4] [5]. Figure 8 is a flow chart that illustrates the general behaviour of the proposed Embryonic system.

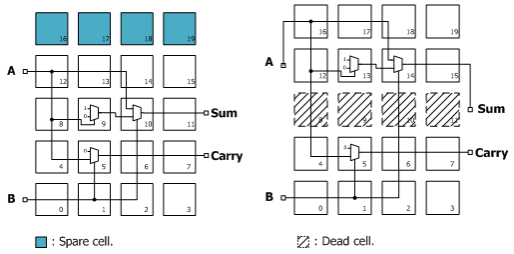

Fig. 7 Half-Adder circuit implemented in an embryonic system with a row-elimination process

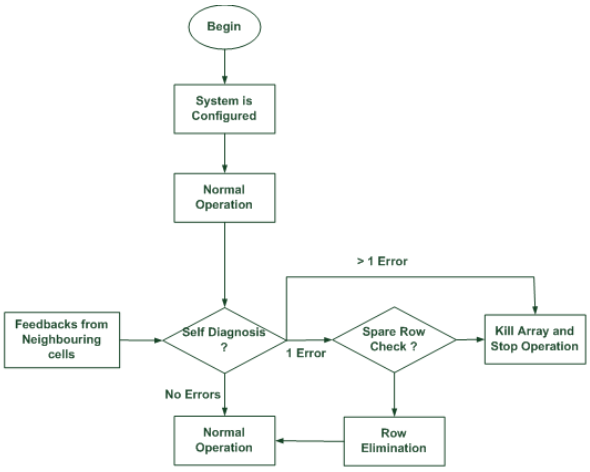

Fig. 8 general behaviour of the proposed Embryonic System

To evolve this complex behaviour, each unit was of the Embryonics cell as in Figure 9 was evolved independently. This is advantageous, as it eases the evolutionary process as well as preventing the requirement to generate a single very complex and very difficult to understand circuit. The employed EA is described in a previous published research by the authors in [12,18].The evolutionary process has successful produced the desired functionalities with a far more superior design circuitry. Details of these results are in [23]

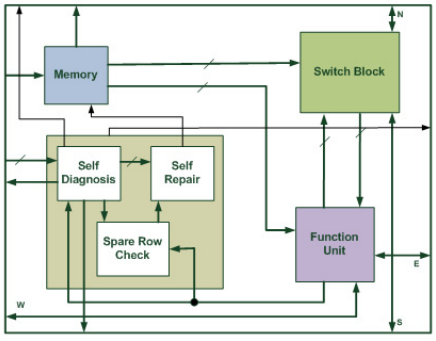

Fig. 9 Functional Blocks of the proposed Embryonics cell

Based on the generated results, it appears that for the Embryonic cell to function as desired, it would only require around 150 gates. This is a significant achievement compared to the cell model proposed in [21], which requires approximately 1000 gates. The authors are aware that the cell model of [21] also implements cell elimination as another mechanism for additional fault-tolerance, but still the difference in gate-count is so huge that it is hard to imagine that adding this functionality would require the difference in gate count between the two cell models. It is also very important to mention the fact that designing the proposed Embryonic cell automatically using EE would save the designer a great deal of time learning, writing and debugging VHDL codes, which is normally a difficult and a time-consuming process.

6. Conclusions

This paper presents the authors' recent research in the area of EHW and/or EE. While online evolution is the ultimate aim of EHW for adaptive fault tolerance, the presented research is mainly focused on offline evolution for design synthesis of electronic systems, which practically demonstrates the concept of *evolvibility*. The first part of the paper presented important cases studies where EE could capably uncover novel and more efficient topologies of real world applications of both analogue and digital electronic systems. The application of EE in analogue systems using multi-objective EA, presented in section 4, is believed to be unprecedented and it outperformed previously published results using single objective EA. The second part of the paper presents an unprecedented research effort where the EE approach is employed for autonomous synthesis for an Embryonics system. The obtained design of the proposed Embryonis cell, in addition to being highly intuitive, was significantly superior compared to an equivalent cell model designed by a human expert, in terms of gate count. This work expands the boundaries of EE to touch on a novel research axis in the broader area of biologically inspired hardware systems. This work lies at the intersection between the Ontogeny and Phylogeny of the POE model propose in [24]. An Embryonics system which is evolvable is indeed a two-in-one approach to enhanced fault tolerance. Furthermore, being intrinsically, a self-repair system overcomes one of the known disadvantages of EE that is maintainability.

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