

Test Time Reduction of 3D Stacked ICs using Ternary Coded Simultaneous Bi-directional Signaling in Parallel Test Ports

Iftikhar A. Soomro, Mohammad Samie, and Ian K. Jennions

Abstract—In order to meet the increasing demand for more performance with reduced power consumption and chip form-factor, semiconductor manufacturing is moving towards 3D Stacked Integrated Circuits (SIC). One of the challenges in bringing this technology into realization is the complicated test accessibility requirements of 3D chips, which apart from having adequate defect coverage, should also have minimal test time. A major limiting factor in test time improvement of ICs is the number of chip terminals, such as pins or Through Silicon Vias (TSVs) available for bulk vector transport in testing. In the conventional design, a chip terminal is only used to either send or receive data at any given time. In this paper, a test accessibility architecture based on ternary encoded Simultaneous Bi-Directional Signaling (SBS), intended for use in parallel Test Access Mechanism (TAM) in System on Chip (SoC) based designs, is proposed. This method enables the use of chip terminals to simultaneously send and receive test vectors, effectively doubling the per-pin efficiency during testing. Experiments show that this technique reduces the Overall Test Time (OTT) by up to 53.6% as compared to conventional TAM design methods.

Index Terms— 3D Stacked Integrated Circuits, System on Chip, Design for Testability, Simultaneous Bi-directional, Test Access Mechanism

I. INTRODUCTION

WITH advancement in manufacturing technology, electronic devices are miniaturizing at an exponential pace. The transistor density had continued to increase with smaller technology nodes; however, further scaling, as per Moore's law, seems to be difficult owing to performance and power concerns [1]. One of the promising ways forward is by forming 3D Stacked Integrated Circuits (SICs), in which the individual dies are stacked vertically and interconnected using Through Silicon Vias (TSVs), micro-bumps or wire bonds, before being packaged as a single chip, as illustrated in Fig. 1.

This allows more functionality to be embedded with a reduced footprint and also addresses another critical problem being observed in 2D designs, that of increasingly long interconnects and latency issues. This concept is already beginning to gain attention in processor design [2], multi-core processors with stacked memory [3], FPGAs [4] and chips have been manufactured by leveraging the third dimension, such as DDR 3 memory ICs [5].

The test time of ICs increases with design complexity and node density and has been a subject of significant research over the years. A significant contributor to test time is the test vector transport phase in which a large volume of data is required to be serially shifted into the internal scan-chains [6]. 3D stacking brings about several additional and more complex challenges for test access [7][8][9][10]. First, higher transistor density increases the probability of manufacturing defects such as metal bridging, metal opens, via opens and transistor defects. It therefore, requires higher test vector volume for adequate coverage but without any significant increase in the chip terminals which further tightens the test access bottleneck. Second, the manufacturing process of 3D SICs introduce additional defects and necessitates multiple test instances. Apart from wafer level and chip-level testing (known as pre-bond and post-bond testing respectively), the 3D SIC has to be tested at every point during the stacking process, known as mid-bond testing. Finally, the limited number of inter-die vertical connections (such as Through Silicon Vias (TSVs), micro-bumps or wire-bonds) add a further test access restriction in addition to chip terminals when transporting test vectors to dies higher up in the stack. As a result of the stated challenges, the Overall Test Time (OTT) in 3D SICs increase significantly compared to conventional 2D Chips, necessitating new test-access designs to bring down the test time and hence the test cost of the chips. Testing 3D SICs is therefore considered a major constraint and listed as one of the difficult challenges for

I. Soomro, M. Samie and I. K. Jennions are with the School of Aerospace, Transport and Manufacturing, Cranfield University, College Road, Cranfield, MK430AL, United Kingdom (e-mail: i.soomro@cranfield.ac.uk; m.samie@cranfield.ac.uk; i.jennions@cranfield.ac.uk).

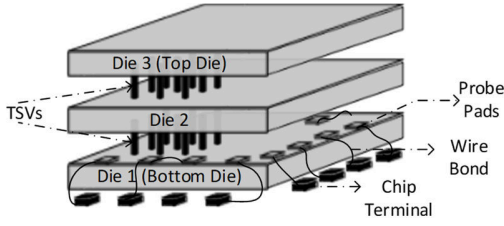


Fig. 1. An illustration of 3D stacking of dies using TSVs

the industry by the International Technology Roadmap for Semiconductors (ITRS) [11].

In this paper, a novel Test Access Mechanism (TAM) design is proposed for 3D SICs that doubles the data transfer efficiency of the pins and TSVs, resulting in a substantial decrease of the test times. This is achieved by leveraging Simultaneous Bi-directional Signaling (SBS) for full-duplex test mode communication at chip terminals. SBS allows transmission and reception of test bits simultaneously compared to the conventional Uni-Directional Signaling (UDS) scheme in which the signal could travel in only one direction at a given time. Using SBS, a complete transmission and reception channel could be formulated using a single electrical path at the chip terminal instead of two, effectively doubling the number of test-channels and increased parallelism in test scheduling. The paper further discusses the TAM design considerations for the incorporation of SBS in 3D SICs such that it does not interfere with the functional mode performance and standard DFT logic, such as JTAG compliant boundary scan registers. An example implementation suitable for low-frequency test vector transportation is presented, and its electrical characteristics are discussed. The performance gains of SBS compared to the traditional TAM design methods have been investigated on previously reported 3D SIC designs based on ITC'02 benchmarks. In this way, the logic level, the circuit level and the application level implications of this approach are evaluated. The proposed design supports scan tests for all test instances (pre-, mid-, and post-bond) in a 3D IC test flow.

The rest of the paper is organized as follows. In Section II and III, the background and prior work are described. In section IV, the SBS based TAM design approach and design considerations are presented. In section V, the circuit design for SBS and Spectre simulations are presented. Test time reduction of SBS compared to UDS in 3D SICs is discussed in section VI. The paper concludes in section VII.

II. BACKGROUND AND MOTIVATION

In VLSI devices, testing is a vital requirement for any IC design to ensure its reliable operation. Testing of a core-based chip design involves three main components: a) The cores and the wrappers, b) a tester which generates required test vectors, controls the test operation, and evaluates test response and, c) a Test Access Mechanism (TAM) which transports the test patterns/ responses between the cores and tester. Scan based testing is the most common way of Design for Testability (DFT) in core-based designs. The functional front end of the chip is designed as usual, and later the Flip Flops are made scan-

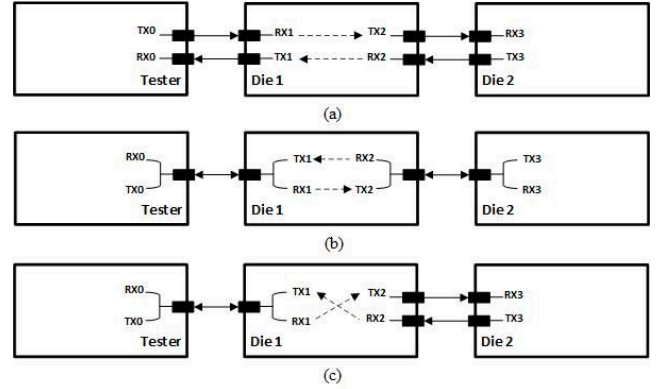


Fig. 2. A single test channel using: (a) Conventional signaling – uses two wires (b) SBS – uses one wire (c) A combination of Uni- and SBS – one wire between tester and Die 1, two between Die 1 and Die 2

test accessible by forming them into shift registers or scan chains using CAD tools. Testing is performed by sending in a set of pre-calculated test vectors to these scan-chains and observing the response.

The scan vectors could be transported to the scan chains in several ways. The simplest being a Serial Test Access Mechanism (STAM) such as IEEE 1149.1 (aka JTAG) [12]. However, JTAG only has a single serial channel, which means that the data has to be shifted one bit at a time, which severely limits its use for high data volume transfer for which a Parallel Test Access Mechanism (PTAM) is used. In a PTAM, such as that allowed by IEEE 1500 Standard [13], a chip's functional I/Os are temporarily used to enable data transfer on multiple test channels in parallel instead of one. It may be noted that the data is still shifted serially through the PTAM but using a higher number of test channels. Here, a 'channel' is defined as a single bit path capable of transporting a test vector to and from the Automatic Test Equipment (ATE) and the core under test. A similar architecture based on a combination of STAM and PTAM is expected for 3D SICs, a standard for which is under development as P1838 Standard [14].

The OTT of an SoC depends primarily on the test data volume (V), scan frequency (s_f) and the available number of test channels (T_{ch}) in a PTAM. A simplified estimate of the OTT can be given by $OTT = V/(s_f \cdot T_{ch})$. Clearly, the OTT decreases with decreasing V and increasing s_f and T_{ch} . The test data volume reduction can be achieved using test compression techniques [6]; however, beyond a certain point, it is likely to come at the cost of reduced fault coverage. The scan frequency is limited by thermal and design constraints; the scan chain insertion is not optimized for performance, and therefore the scan frequency is usually limited to a few tens of MHz. Most of the conventional TAM design methods, therefore, rely on either increasing the number of test channels, which is limited by the chip pins or increasing the pin efficiency by techniques such as TDMA and SerDes [15][16][17][18].

In the conventional TAM design, a test channel is formed using a separate terminal for input and output; therefore the number of test channels in a PTAM is half the available chip terminals, as shown in Fig. 2(a). This is because conventional chip terminals are designed to communicate in simplex (uni-

directional) or half-duplex (bi-directional) configuration. In either case, only a single transmit-receive pair is active at a given time, and the data could only travel in one direction. This simplifies the hardware implementation and has been sufficient in keeping the OTT of medium complexity chip designs down to an acceptable level; however it does not scale well for more complex designs such as 3D SICs which demand a higher number of test channels.

On the other hand, if a full-duplex configuration such as SBS is used in the TAM, the data could be shifted in and out at the same pin simultaneously, as shown in Fig. 2(b), resulting in channel width equal to the number of chip terminals. The parallelism introduced by SBS increases the number of test channels, significantly reducing the OTT. Consider the example of an SoC with two cores and two chip terminals. Each core has a single scan-chain of 50 bits and requires two test patterns (say P1 and P2) for the scan-test. In a conventional TAM design using simplex/ half-duplex chip terminals, the 2 pins would form a 1 bit wide TAM. Consequently, both the scan-chains could be concatenated to form a single channel of $50 + 50 = 100$ bits as shown in Fig 3(a). If however, an SBS based TAM is used, the resulting TAM would be 2 channels of 50 bits each as shown in Fig 3(c). The resulting schedule for both arrangements is shown in Fig 3(b) and (d). Cx-Cy denotes that the cores x and y will be connected in series and Cx||Cy indicates the cores will be connected in parallel to form a test session. It is evident that the OTT in the case of uni-directional TAM with schedule C1-C2 is 300 clock cycles because of a single TAM channel, whereas for SBS TAM with schedule C1||C2, the OTT is only 150 cycles. It could, therefore, be concluded that SBS ports increase the available TAM width, allowing more parallelism which in the case of this example resulted in a reduction of 150 cycles in the OTT.

The added advantage of using SBS is that it can work in conjunction with the conventional TAM, as shown in Fig. 2(c). This means that instead of modifying all chip terminals to support SBS, only the most essential subset causing the bottleneck may be fitted with SBS while the remaining chip terminals operating as usual. This also implies that this method can be used to integrate hard-dies, in which the chip terminals are not modifiable.

III. PRIOR WORK

Most of the previous research has been focused on design, optimization, and scheduling of a TAM aimed at minimizing the OTT while using minimal chip resources. The TAM could connect the cores in series, such that the scan-chains are tested sequentially, or the cores could be connected in parallel such that they could be tested simultaneously. In an ideal situation, all the cores in a die and all the dies in a 3D SIC would be tested simultaneously, in parallel, which would result in the minimum OTT. However, several constraints limit this approach such as: 1) It may not be possible to access all cores at a time due to limitations posed by IC terminals and TSVs 2) there may be limitations of power and thermal dissipation which need to adhere 3) chip area that could be dedicated for the test

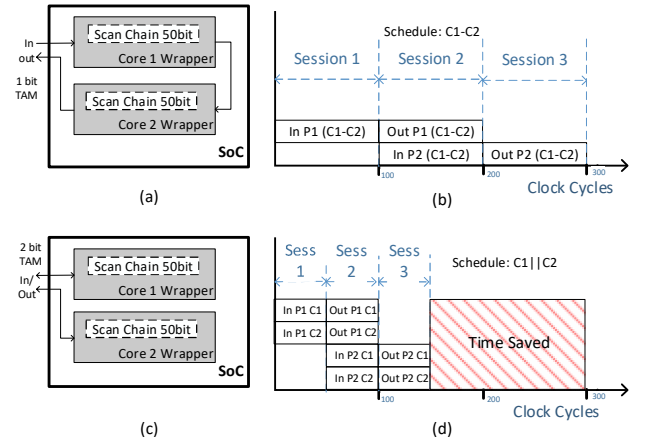


Fig. 3. Conventional vs SBS test ports (a) TAM design for uni-directional port and associated test schedule in (b), (c) TAM design for SBS port and associated test schedule in (d)

architecture may be limited. In System on Chip (SoCs), every core has specific test requirements that are specified by the core designer and it is the job of SoC vendor to put in place an appropriate Test-Access Mechanism (TAM) that fulfills these requirements. Clearly, there is a tradeoff between resources and the test time, and the task of the designer is to find the best possible solution for a TAM.

TAM optimization is shown to be an NP-Hard problem and one way of reducing OTT is to find an improved optimization algorithm that points out the best possible TAM in the entire solution space with the objective of minimizing OTT while adhering to the chip constraints. Most of the noticeable work has been focused on 2D SoC designs and various approaches to solving the problem have been adopted such as Integer Linear Programming [19], Rectangle Bin Packing [20] and heuristics [21] [22]. While most of the work on 2D TAMs has been focused on the constraints imposed by available TAM width, some researchers [23][24] have also focused on thermal and power consideration which is also an important factor since significantly higher switching activity is observed during tests.

As mentioned previously, 3D SICs are considerably different and make the optimization process more challenging [7][8][9]. Wu et al. [25] presented a method to optimize the 3D TAM designed using wrapper design suggested in [19] using a heuristic combination of Integer Linear Programming (ILP), randomized rounding, and LP relaxation. In [26], the authors addressed the problem of scan-chain ordering and partitioning using the Genetic Algorithm and ILP combined with heuristics to reduce wire length and OTT. The authors in [27] proposed heuristics to design optimized TAM under a set of uncertainties. It may be pointed out that the TAM optimization solution space is bounded by the physical layer of the TAM design. Most of the above works have relied upon conventional Uni-directional TAM design techniques and have not proposed any significant improvements in the physical design of the access infrastructure itself, more specifically, the improvement in pin efficiency.

The works that involve improvement of pin-efficiency include using Time Division Multiplexing (TDM) [15] [16]. The work in [15] has been concerned with reducing access time

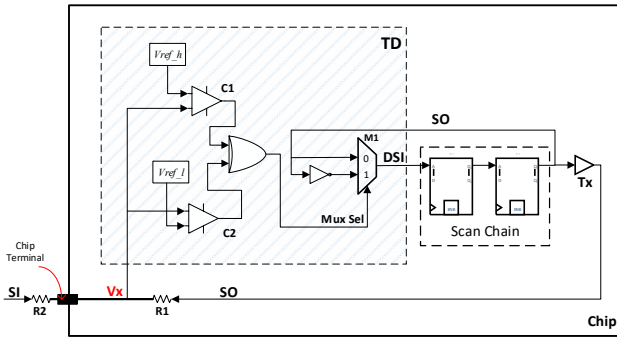


Fig. 4. Test Channel for a 2 bit Scan-Chain using Ternary Encoding and Decoding at the Chip Terminal

for serial Reconfigurable Scan Networks (RSNs). The authors in [16] proposed a TDM based method to reduce the overall test time of 3D SICs. The data is loaded through parallel buses at the scan frequency and is then serialized. The serial data can then be transferred from one die to another through TSVs operating at higher frequencies. Time de-multiplexers at the receiving end perform the serial to parallel conversion, and the data is shifted into scan-chains at the scan frequency. Another approach to allow optimal utilization of tester resources was presented in [17] and [18]. In [17], the authors introduced the concept of virtual TAMs to efficiently utilize tester resources. Instead of operating the tester channels at a lower frequency to match scan frequency, Serializer and De-serializer (SerDes) were used to enable high-frequency data transfer between ATE to SoC I/O and low-frequency operation at the scan chains, thus maximizing ATE resource utilization. The approach adopted in this paper focuses on Simultaneous Bidirectional Signaling (SBS) at the chip terminal which internally presents two virtual unidirectional I/Os to the SoC, just like UDS. The test time reduction techniques mentioned above could be designed on top of these virtual I/Os providing further test time reduction, with an added advantage that SBS would require one pin, whereas UDS would need two.

The idea of SBS was initially reported in [28], following which improved designs capable of delivering up to 900Mbps and 8Gbps (450Mbps and 4Gbps in either direction, respectively) were proposed and tested on fabricated devices in [29] and [30]. While these works rely on voltage-mode signaling, further enhanced design using current-mode differential transceivers were proposed in [31][32][33] for improved power efficiency in off-chip (chip to chip) [31][32] as well as on-chip (core to core) [33] signaling. In 3D SICs, SBS through TSVs has different design requirements, primarily because of negligible path resistance when compared to off-chip communication. The authors in [34] presented an SBS transceiver design for vertical communication in 3D SICs through TSVs and achieved a data rate of 9.1Gbps. The performance of a single SBS channel has been shown to be better than two UDS channels both in terms of power as well as the on-chip area [29][34]. The decrease in power consumption is attributed to lower switching activity as well as reduced voltage swing in SBS.

The research in SBS has mostly been focused on functional communication at higher data rates. High-speed SBS is usually complicated by noise concerns such as common-mode noise rejection, echo cancellation, EMI considerations and tight control of threshold voltage and comparator tolerances. However, as mentioned earlier, scan frequencies are typically a few tens of MHz, for which the design considerations become much relaxed, making testing a very viable application of SBS. The difference, however, is that unlike single-ended chip to chip channels where communication takes place between two transceivers, in this case, the chip terminal needs to be capable of functional communication in normal mode (assuming it is UDS) and SBS in test mode. To the best of our knowledge, TAM design methodology in 3D SICs using SBS has not been studied in the past.

IV. PROPOSED APPROACH

Simultaneous Bi-directional signaling could be made possible by using ternary level encoding at the chip terminals (Pins and TSVs). The output from the sender and receiver is encoded into the ternary level at the chip terminal and a decoding circuitry is used to convert back to binary levels. Here it may be noted that the chip-terminal could either be the chip pin (only in case of the die which connects to the PCB, mostly the lowermost die) or a TSV. It is assumed that the functional communication at the chip terminal is UDS and the proposed design aims to add SBS capability specifically for use in the test mode.

A. Ternary Level Coding

The overall idea is illustrated in Fig. 4 using an example chip with a single scan chain comprising of two FFs. The output of the scan chain is denoted as Scan Out (SO) and is fed to the chip terminal using an inverter as a transmitter (Tx), which becomes active during SBS mode. The external end of the chip terminal is to be driven using a similar setup (not shown in the figure) in another die (in case of TSVs) or the tester (in case of the first die) and is denoted as Scan In (SI). Two series resistors of equal value $R1$ (located on-chip) and $R2$ (on tester/another die) form a voltage divider circuit and essentially encode the binary input signal into the ternary level Vx at the node X. It may be noted that the resistors $R1$ and $R2$ are explicitly shown for clarity; in actual implementations, the SI and SO line driver output impedances and the I/O cell resistance may be sufficient to form the voltage divider circuit. The encoded signal is denoted as Vx , and it could take three values 0 (Vxl), Vdd (Vxh) or $\frac{1}{2} Vdd$ (Vxm) depending on if SI and SO are both low, high or in opposite states respectively.

The Ternary Decoder (TD), shown in the hatched block, receives a copy of the SO signal, which is tapped just before the Tx where it remains in the binary state. The other input to the TD is the ternary encoded signal Vx , which is fed to one of the inputs to the two voltage comparators $C1$ and $C2$. The second input of the comparators is connected to high voltage reference $Vref_h$ and low voltage reference $Vref_l$, which in this case are taken to be $\frac{2}{3} Vdd$ and $\frac{1}{3} Vdd$ respectively. If Vx is 0 or Vdd , both comparators produce the same output (0 or 1) and if Vx is

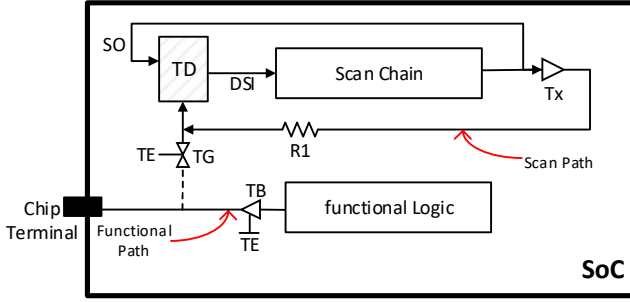


Fig. 5: Test and Functional mode isolation (in this illustration, the chip terminal is a functional output)

equal to $0.5 V_{dd}$, C2 produces a 1 (since $1/2 V_{dd} > 1/3 V_{dd}$) and C1 produces a 0 (since $1/2 V_{dd} < 2/3 V_{dd}$). The outputs of C1 and C2 could be fed to an XOR gate which in turn controls a 2 to 1 Multiplexer M1. One input of the Multiplexer M1 receives the SO signal while the other input received an inverted copy of the SO. The output of the Mux is the output of the Ternary Encoder and is denoted by Decoded Scan In (DSI) signal which is the input to the Scan Chain. The DSI always takes on the same value as SI, simply by deciding whether it is the same as SO or the opposite, depending on the Mux Sel signal from the XOR gate. In this way, the transmission and reception of the signal could be achieved simultaneously.

B. Test and Functional mode isolation

As mentioned previously, the use of SBS signaling in testing is complicated by the requirement of usability of the chip terminals in the functional operation of the chip as well. The design of the SBS must take into consideration that the functional path, which could be required to operate in the GHz range, may not be affected by the presence of SBS mode connections. Therefore, a Transmission Gate/ Analog Switch (TG) is inserted just before the TD on the ternary encoded signal V_x and the drivers or the receiver at the functional side is designed as a Tristate Buffer TB. These switches are controlled by the Test Enable (TE) signal of the Chip, which could either be provided externally through a dedicated chip terminal or could be sourced from the die-level JTAG IR decoder by loading an appropriate user-defined instruction via the TAP controller. The overall arrangement is illustrated in Fig 5. In this case, TE is de-asserted, and TG isolates the test side (dashed line) while TB is active allowing the normal operation of the functional side (solid line). On the contrary, when TE is asserted, the functional side will be isolated.

C. Integration with Boundary Scan

JTAG is a widely used DFT feature that allows essential test accessibility features at all levels of system hierarchy, such as die, chip, circuit board, and system level. Boundary Scan Registers (BSR) is an essential component of JTAG, which allows the observability and controllability at the chip pins for test and debug purposes. Therefore, it would often be necessary to ensure that the incorporation of SBS does not affect the boundary scan capability of the chip. An illustration of an observable and controllable Boundary Scan Cell (BSC) (using an example implementation given in [12]) is shown in Fig 6(a).

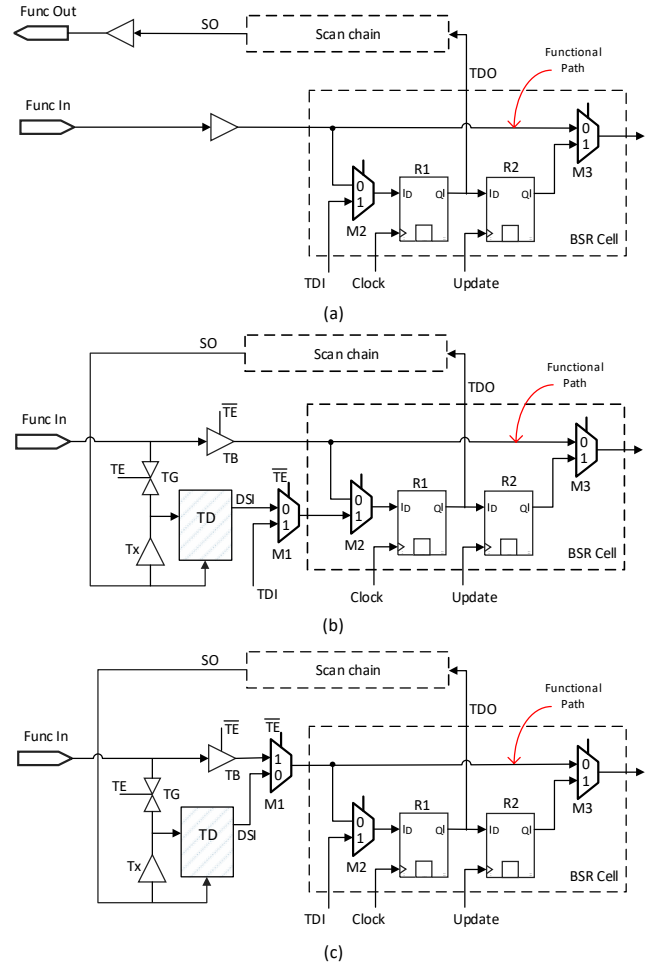


Fig. 6: Boundary scan compliant fully observable and controllable boundary scan cell [12] shown in the dashed box (a) without SBS (b) SBS integration outside functional path (c) SBS integration inside functional path

The proposed incorporation of SBS for a functional pin (in this case an input) could be achieved as shown in Fig. 6(b). As with the non-boundary scan chip terminal (Fig 5), tri-stated buffer is used as a receiver along with TG for isolation. A Multiplexer M1 is inserted between Test Data In (TDI) of the JTAG and R1 flip-flop of the BSR, such that depending on the state of control signal TE, either conventional boundary scan is selected (TE is low) or SBS is selected (TE is high) as shown in Table I. The state of the multiplexers M2 and M3 will depend on the current instruction in the JTAG IR. This configuration supports all the functionality of a conventional BSR, such as normal function, EXTEST, INTEST, SAMPLE, and PRELOAD, with an added option of SBS to support Parallel INTEST (for example when using WPPs of the IEEE 1500 standard compliant core wrappers).

It may be noted that the implementation, shown in Fig. 6(b), does not add any logic in the functional path and does not incur any additional penalty on functional mode performance. However, this comes at the cost of increasing the scan-chain length by 1 bit, as the BSR Cell must be a part of the scan chain. An alternate arrangement is shown in Fig. 6(c) which excludes the BSR from the scan chain while retaining all the functionality of Fig. 6(b). However, it necessitates the inclusion

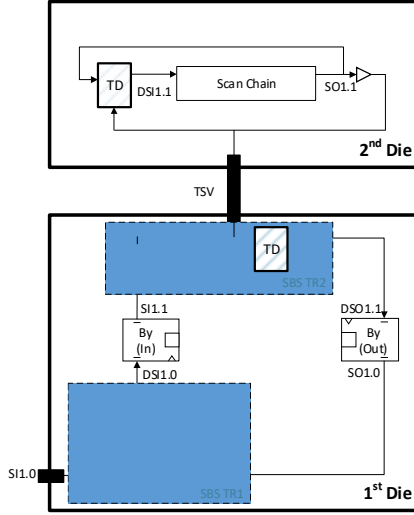


Fig. 7: An illustration of SBS for accessing higher dies in a 3D SIC through TSVs

TABLE I
MODE CONFIGURATION STATES

Mode	TE	TB	TG	M1
Function	0	HiZ	Open	X
JTAG	0	HiZ	Open	TDI
INTEST SBS	1	Drive	Closed	DSI

of the multiplexer M1 in the functional path which may affect the functional mode performance. If the performance degradation is acceptable, the arrangement in Fig. 6(b) is preferable because SBS can now be used for both functional and test mode communication along with UDS. Moreover, both these implementations also ensure that in case of a defect in the SBS circuitry, the testing could still be performed using conventional UDS based DFT resources, thus providing redundancy.

D. Vertical Access Considerations in mid- and post-bond testing

As mentioned earlier, SBS implementation through TSVs is different in terms of transceiver design characteristics due to the low resistance and high capacitance of the TSV path. Therefore, further considerations are required for overall TAM design when accessing the higher dies through the first die. Consider, for example, the case in which the signal is required to be transmitted to the second die from the chip terminal of the first dies as illustrated in Fig. 7. In this case, the Ternary Encoded signal at the chip pin is required to traverse through more than one SBS Transceiver (SBS TR). The input signal SI1.0 at the 1st die pin must travel through the SBS TR1, followed by the SBS TR2 to reach the second die, while at the same time the scan-out signal SO1.1 at the second die must travel to the chip pin in the opposite direction. It is clear that the signal traversal path may induce delays which may become excessive when accessing dies which are further up in the stack. Therefore bypass flip-flops must be inserted to ensure that the signal does not degrade when passing through multiple dies. The additional

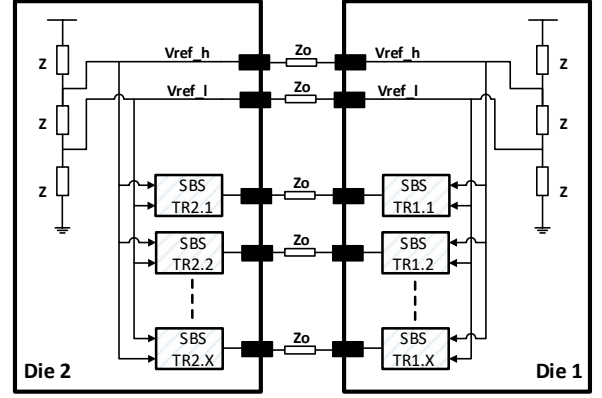


Fig. 8. Reference Sharing

flip-flops ensure that the signal only propagates through one die at a time utilizing a full clock cycle. This problem is not specific to SBS and is relevant to any TAM design. The standard DFT practice for 3D SICs is expected to include mid-way flip-flops in the PTAM to avoid signal integrity issues altogether [14]. Fig. 7 shows the bypass flip-flops inserted in the scan in (By In) and scan out (By Out) paths, respectively. The addition of the flip-flops results in an increase in the scan path length for Die 2 and onwards depending on the position of the die in the stack.

In order to calculate the test time of the cores in 3D stacked dies using SBS, the equation for core test time calculation of 2D SoCs given in [35] can be extended to stacked dies with DBRs. The test time of the core T_c is then given by:

$$T_c = (s + \max\{s_i, s_o\}) \cdot p + \min\{s_i, s_o\} + s - 1 \quad (1)$$

Where s is the position of the die in the stack, s_i and s_o represent the longest scan-in and scan-out chain lengths of the core wrapper, respectively, and p is the total number of test patterns required by the core. This effects the test time of every core in the SIC except the first die in which case $s = 1$, and the equation reduces to $T_c = (1 + \max\{s_i, s_o\}) \cdot p + \min\{s_i, s_o\}$ which is the same as given in [35] for 2D SoCs.

E. Pre-bond testing

The case of TSV accessible dies is complicated due to difficulty in probing the TSVs at the pre-bond stage. Current processes are capable of producing TSVs with pitch and diameter of less than $5\mu\text{m}$ [36][37][38], which is too small to be accessed through tester probes. Although a die may contain hundreds of TSVs, due to the stated probing issues, only a small subset of TSVs may be made accessible at the pre-bond stage using sacrificial probe pads. Therefore, the problem of pre-bond testing of TSV accessible dies can be considered similar to the pin accessible dies. The TAM design problem for the pre-bond testing may only be required to ensure the maximal utilization of SBS resources in all test instances (pre- mid- and post- bond).

F. Reference Sharing

The comparators C1 and C2 of the Ternary Decoder shown in Fig. 4 require a high and low reference voltage (V_{ref_h} and V_{ref_l}). For low-frequency applications, the dies can have

separate references generated locally on the die or sourced through the tester. However, for high-frequency applications, in order to couple the common mode noise to the receivers as well as to cancel out the effect of power supply variations, it may be necessary to have a shared reference between the dies, as shown in Fig. 8.

The requirement of two wires for reference generation between the first die and the tester, and between the dies also reduces the number of test pins and TSVs available for the transportation of the test vectors. If the number of available test pins is denoted by P_{max} and the total number of TSVs in the entire stack is given by TSV_{max} , then the pins available for testing (W_{bi}) and TSVs available for testing (TSV_{bi}) using SBS is given by:

$$W_{bi} = P_{max} - 2 \quad (2)$$

$$TSV_{bi} = TSV_{max} - 2(M - 1) \quad (3)$$

Where M is the number of dies in the stack. Despite the reduction in test pins and TSVs in the SBS scheme, the number of test channels increases significantly compared to the conventional uni-directional approach since a single wire forms a channel in the former approach, whereas two wires form one channel in the latter approach.

V. SBS TRANSCIVER CIRCUIT DESIGN

In this section, an example SBS Transceiver (SBS TR) design is presented for use in low-frequency test mode for 3D TSV communication. There are several ways in which SBS can be implemented. For high-frequency applications, differential mode communication is used [39] [40]. Although differential mode transceivers are power efficient and highly noise resistant, allowing very high bandwidth, the requirement of two pins to form a channel limits its use in Parallel Test Ports, for which single-ended transceiver designs [34][41][42] is preferable.

As mentioned earlier, the above works are designed for normal mode communication for high-speed data transfer. The implementation discussed below is intended to be used as an additional circuit for used in test-mode such that a) the effect on functional performance is minimal b) Given the low-frequency requirements, the implementation is simplified and power efficient.

The main components of an SBS implementation shown in Fig. 9(a), where SBS communication takes between the 2nd Die and the 1st Die through a TSV. The Transmitter and the Ternary Decoder (TD) in both dies are similar; therefore, the detailed schematic is shown only for the 2nd die. In the following paragraphs, the circuit design is described in light of the different design options.

A. Transmitter

The transmitter can simply be designed as an inverter of appropriate size to allow the required bandwidth. However, this design may not be power efficient when the driving transmitters at either end of the channel are in opposite states, consuming static power, as reported by the authors in [34]. To limit the static current, the proposed transmitter is built as an inverter

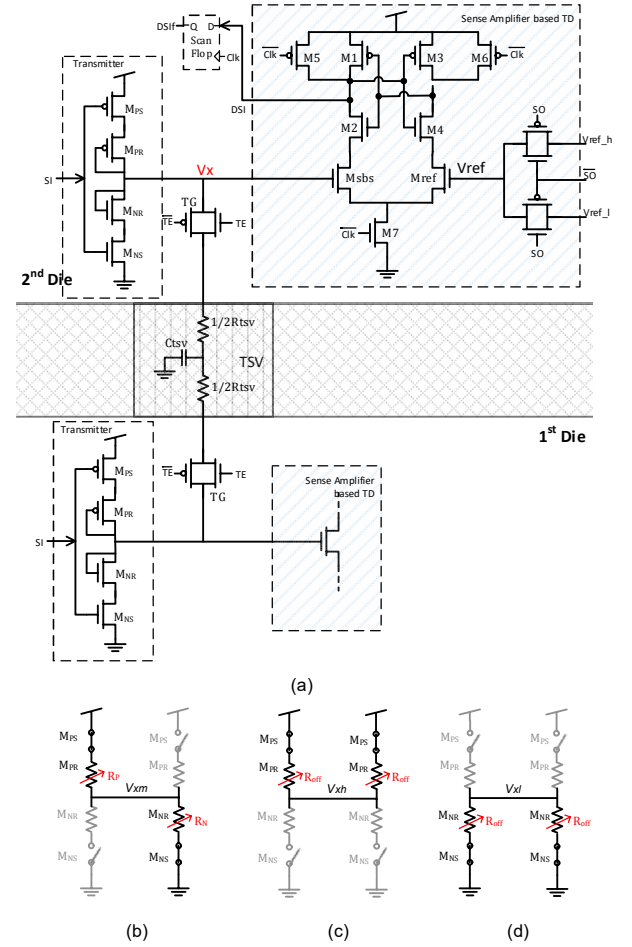


Fig. 9. (a) Proposed SBS Transceiver Circuit (b) equivalent circuit for V_{xm} (c) equivalent circuit for V_{xh} (d) equivalent circuit for V_{xl}

with diode-connected MOSFETs as shown in Fig. 9(a) [31]. The MOSFETs M_{NS} and M_{PS} perform the inverter switching and the diode-connected MOSFETs M_{NR} and M_{PR} serve as active series resistors, minimizing the static current and hence the static power consumption. Similar to a normal inverter, there is no static power consumption when the transmitters at both ends are either high or low.

The resistance of the diode-connected MOSFETs at a given instance is a function of V_x , and consequently the state of both the transmitters (11,10,01,00). Fig. 9(b) shows the equivalent circuit for the middle voltage level (V_{xm}) when one of the transmitter is high and the other is low (10, 01). Ignoring the TSV resistance and assuming the switching transistors as ideal, the middle voltage level $V_{xm} = V_{dd}(R_P/(R_P + R_N))$ where R_P and R_N are the resistance of M_{PR} and M_{NR} at $V_x = V_{xm}$. The resistance R_{on} of a diode-connected MOSFET can be approximated by:

$$R_{on} = \frac{V_{DS}}{I_d} \text{ where } I_d = \mu C_{ox} \frac{W}{L} (V_{GS} - V_t) V_{DS} \quad (4)$$

therefore,

$$R_P = \frac{L_p}{\mu_p C_{ox} W_p (V_{xm} - V_{t(p)})} \quad (5)$$

$$R_N = \frac{L_n}{\mu_n C_{ox} W_n (V_{xm} - V_{t(n)})} \quad (6)$$

Where L and W are the length and width of the diode-connected MOSFETs, μ is the mobility of the channel, C_{ox} is the oxide thickness, and V_t is the threshold voltage. It is clear that the W and L ratios of the diode-connected NMOS and PMOS can be adjusted to obtain the desired V_{xm} level. When both the transmitter inputs are low (00), as shown in Fig 9(c), V_x is pulled high through the M_{PS} and M_{PR} , however as V_x approaches V_{dd} , M_{PR} enters into the sub-threshold region and the resistance R_{P1} approaches the off resistance R_{off} , restricting the upper voltage swing to $V_{xh} = V_{dd} - V_{t(p)}$. Nevertheless since there is a small conduction current in the cut-off region as well, V_x will gradually approach V_{dd} and hence $V_{dd} \geq V_{xh} \geq V_{dd} - V_{t(p)}$. Similarly, when both the transmitters are sending high (11), V_x is pulled low to $V_{xl} \leq V_{t(n)}$ as shown in figure 9(d). The upper and lower voltage swing can be further improved by using body effect to reduce V_t .

In Fig 9(a) the transmission gate switch TG added after the transceiver ensures that the transceiver does not affect the normal mode operation (TG is open when $TE=0$). However, the diffusion parasitic capacitances of TG do appear in the functional path, but it is minimal compared to the TSV capacitance, and the effect on normal mode performance is expected to be negligible.

B. Ternary Decoder

The main component of the ternary decoder is the voltage comparator which could be designed either as a differential amplifier [41] or a voltage-sense amplifier [34]. The proposed receiver has been based on the later, because of its simple design, robustness, and low power consumption. The circuit diagram of the sense amplifier based TD is shown in Fig. 9(a) Note that the TD in Fig. 4 contained two comparators, an XOR gate and a multiplexer, however for area and power efficiency the proposed implementation is optimized such that the XOR gate and the multiplexer isn't required and only one comparator is used and the reference is switched between the high value ($Vref_h$) and low ($Vref_l$). When the scan-out signal is high ($SO=1$), the transmitter output is low and the signal V_x can only take the low and middle value and vice-versa. Therefore, the lower reference $Vref_l$ is selected when $SO=1$ and $Vref_h$ when $SO=0$. The reference switching is achieved using the transmission gate multiplexer with SO as the control signal.

The sense amplifier receives the ternary encoded input V_x and the reference voltage $Vref$ at the gates of NMOS transistors M_{sbs} and M_{ref} , respectively. The transistor pairs $M1, M2$ and $M3, M4$ form two cross-coupled inverters, forming a regenerative latch. The sensing takes place during the positive half cycle. The transistors M_{sbs} and M_{ref} , depending on the voltages at the respective gates, will have different on-resistance and hence the voltage drop. In the negative half cycle, one of the nodes of the regenerative latch with the higher voltage is pulled high, and the lower voltage is pulled low, hence the comparator action. Since the input to TD was inverted by the transmitter, the inverting output of the sense-amplifier is taken as the output DSI , which can be fed directly to the scan

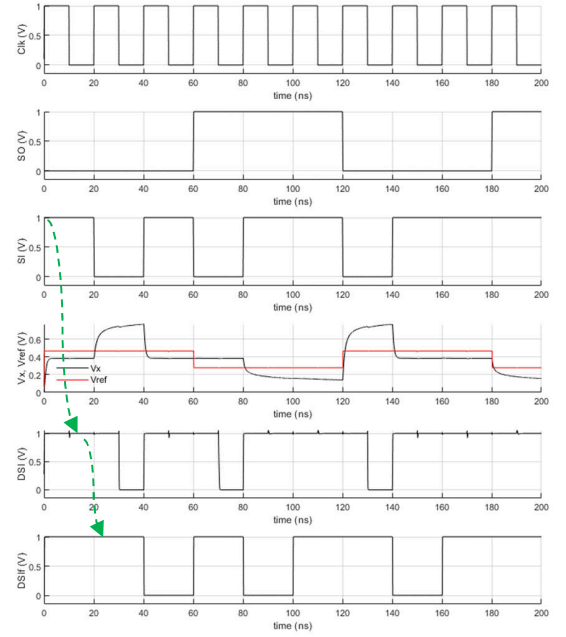


Fig. 10. Simulation results of the various signals in the proposed SBS Transceiver Circuit in Fig. 9. (Vertical scale normalized to V_{dd}).

TABLE II
AVERAGE POWER CONSUMPTION (IN μW)

	UDS	SBS	Diff (%)	SBS*	Diff* (%)
Transmitter	6.82	10.3	50.9	7.08	3.71
Receiver	2.61	1.76	-32.8	1.77	-32.37
Total	9.43	12.06	27.77	8.85	-6.28

*Transmitter turned off for the negative half cycle of the clock

chain. The transistors $M5$ to $M7$ are controlled by the clock and allow the latch action.

The proposed TD behaves like a neg-edge triggered flip-flop and introduces a delay of one clock cycle; however, it removes the requirement of a separate flip-flop required for Die-to-die communication, as shown in Fig. 7. As noted earlier in Sec. IV(D), the inclusion of the flip-flops is necessary from the DFT standpoint and is expected to be a part of the upcoming 3D IC DFT standard P1838 [14].

C. Simulation results

The SBS Transceiver was simulated with Cadence Spectre using 180nm technology. The design was limited to 50 MHz frequency which was easily achieved by using minimum size for all transistors in the transceiver. Assuming a TSV with $5\mu m$ diameter, $20\mu m$ length, substrate doping concentration N_a of $2 \times 10^{15}/cm^3$, and Oxide Thickness of 200nm, the TSV was modeled based on [43] as a lumped RC circuit with a resistance $R_{tsv} \approx 100m\Omega$ and capacitance $C_{tsv} \approx 30fF$ as shown in Fig. 9. The series inductance of the TSV was ignored as it is negligible at low frequencies. Minimum sized transistors provided a V_x swing with $V_{xh} \geq 0.7V_{dd}$, $V_{xm} \approx 0.39V_{dd}$, and $V_{xl} \leq 0.2V_{dd}$. $Vref_l$ and $Vref_h$ were chosen to be $0.28V_{dd}$ and $0.47V_{dd}$, respectively. The voltage levels at various points for the four

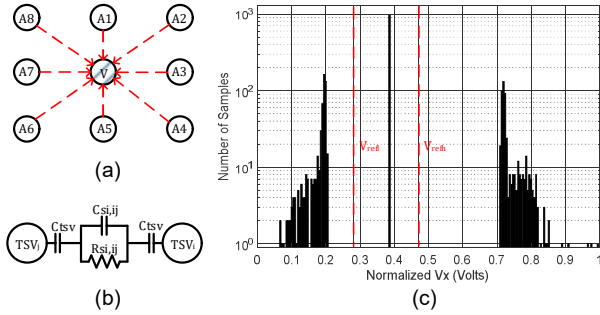


Fig. 11. TSV Cross-coupling (a) Victim TSV (center) and 8 aggressor TSVs in a 3x3 Cluster (b) TSV-TSV Coupling model [44] (c) Histogram of V_x voltage levels at the receiver sampling time, under cross-coupling.

possible combinations of SI and SO are shown in Fig. 10. The output, DSI , of the Ternary Decoder correctly reproduces the Scan-In (SI) signal and appears at the output of the first scan-flop ($DSIf$) with a delay of 1 clock cycle.

The power consumption of the proposed SBS transceiver was compared with the unidirectional transceiver designed as 4x-buffers. The average power consumption for a pair of transceivers (one channel), when transmitting and receiving the same Pseudo-Random Binary Sequence (PRBS), is given in Table II. The SBS transceiver consumes approximately 27% more power compared to UDS. However, it may be noted that the TD samples the V_x at the negative edge of the clock cycle; therefore, one of the TG (hence the transmitter) can be turned off during the remaining (negative) half cycle of the clock, further reducing static power. This can be achieved with a NOR gate with $\overline{Clk}$ and $\overline{TE}$ as the inputs, whose output (and a complement, generated using an inverter) controls the TG . In this case, the SBS transceiver consumes approximately 6% lesser power compared to UDS (inclusive of the power consumed by the added circuit), at the expense of 6 additional transistors per channel.

TSVs are usually designed in clusters, and so, cross-coupling with the neighboring TSVs is an essential concern in TSV communication. The performance of the SBS transceiver in the presence of noise coupling was studied assuming a 3x3 TSV cluster with the center TSV as the victim as shown in Fig 11(a). Considering $10\mu\text{m}$ pitch between TSVs and silicon resistivity of $6.89\ \Omega\cdot\text{cm}$ (for $N_a=2\times 10^{15}/\text{cm}^3$), the values of the coupling capacitances $C_{si,ij}$ and resistances $R_{si,ij}$ of the silicon substrate between the victim TSV i and aggressor j were calculated using the coupling model described in [44], as shown in Fig 11(b). Assuming all the aggressors are being driven by similar SBS transceivers with different PRBS (for a $40\mu\text{s}$ simulation period), the histogram of the ternary encoded signal V_x at the receiver sampling time (negative clock edge) is shown in Fig 11(c). Given the low frequency of operation, almost all the couplings are eliminated during the positive half-cycle, before it is sampled by TD at the negative clock edge. In all cases, V_x remains stable at approximately $V_{xm}\approx 0.39V_{dd}$, $V_{xh}\geq 0.7V_{dd}$ and $V_{xl}\leq 0.2V_{dd}$. Also, as the drain current is not ideally zero in the sub-threshold regions, V_{xh} and V_{xl} will slowly tend to approach V_{dd} and G_{nd} respectively. This explains the signal

TABLE III
3D SICs COMPOSITION

SIC No.	No. of Dies	Composition of each SIC
1.	5	p93791,p34392,p22810,f2126,d695
2.	5	d695,f2126, p22810, p34392, p93791
3.	5	f2126, p22810, p93791, p34392, d695
4.	2 to 9	p93791,p34392,p22810,f2126,d695, q12710,h953,g1023,d281

spread above V_{xh} and below V_{xl} , caused when the input of both transmitters does not change over consecutive cycles and augmented by the cross-coupling. Sufficient voltage margins exist between V_{ref} and V_x to account for the process variation (TD requires as little as 40mV difference between V_x and V_{ref}). The transceiver operation was also verified across all process corners in the presence of noise coupling.

Overall, at the expense of only 19 minimum sized transistors per TSV, up to 53.6% reduction in test time could be achieved as detailed in the next section. Moreover, separate die-bypass flip-flops may not be required as the TD acts like a flip-flop.

VI. OVERALL TEST TIME COMPARISON

SBS doubles the bandwidth of the channel for a given clock frequency compared to UDS. This statement may be sufficient to report the improvement expected in normal mode communication in which the exact usage of the link over a longer period may not be known. However, testing is a complete process in which the link utilization over the entire period of the test is known, and it is possible to calculate the exact improvements in test times. The overall reduction in test time would depend on the number of available test pins and TSVs, the construction of the SIC and the dies, their test requirements and also the TAM, which may be different for both. In this section, the test time improvements of SBS versus UDS are quantified for various 3D SIC designs reported in the literature for a varying number of pins, TSVs, and the number of dies.

A. TAM Design Methodology

In order to compare the test time of the conventional UDS TAM with SBS (assuming all pins and TSVs support SBS), experiments were conducted using 3 x handcrafted 3D SICs from the ITC 02 [45] Benchmarks reported in [46] and a fourth SIC in which the number of dies was gradually incremented from 2 to 9. The composition of each SIC is shown in Table III. The optimal TAM design and test schedule for both were obtained using ILP, based in part on the model presented in [19] for Test-Bus architecture based die level TAM design [47], and on [46] for 3D SIC TAM design. The optimization problem using ILP is known to be NP-Hard [48] and the complexity increases exponentially with an increasing number of variables and constraints. Therefore, for better runtime efficiency, first the optimal solution for all possible values of the die test time for different TAM widths were pre-calculated using the enumerative method $P_{NPAW_enumerate}$ described in [19]. This was followed by 3D TAM design using the ILP model described in

TABLE IV
TEST TIME COMPARISON FOR SIC 1 USING UNI- AND SIMULTANEOUS BI-DIRECTIONAL SIGNALING

Pins (P_{max})	TSVs (TSV_{max})	Uni-directional			Simultaneous bi-directional			% OTT improvement (uni- vs bi-directional TAMs)
		OTT (cycles)	Schedule	Channel Allocation	OTT (cycles)	Schedule	Channel Allocation	
20	200	5632583	1 3-2-4 5	10;7;3;9;1	3211831	'1-2-3 4-5'	18;18;10;8;18	42.98
30	200	3781790	1-2-3 4-5	12;11;3;4;15	2077911	'1 4-2 3 5'	23;19;8;5;1	45.05
40	200	2854606	1-2 3 4-5	20;14;6;18;2	1541512	'1 2-3 4 5'	24;14;20;16;2	46.00
50	200	2271852	1-2 3 4-5	25;14;6;5;25	1232343	'1 2 3 4-5'	23;14;6;5;48	45.76
60	200	1929521	1 4-2 3 5	25;20;9;5;1	1022692	'1 2 3 4-5'	28;17;7;6;48	47.00
70	200	1643683	1-2 3 4 5	34;20;8;7;1	863264	'1 2 3 4 5'	33;19;8;7;1	47.48
80	200	1455507	1-2 3 4 5	20;11;5;4;25	774276	'1 2 3 4-5'	37;23;10;8;48	46.80
90	200	1314573	1 2 3 4-5	22;12;6;5;25	696956	'1 2 3 4 5'	41;26;10;9;2	46.98
100	200	1167503	1 2 3 4 5	24;14;6;5;1	629794	'1 2 3 4 5'	45;30;11;10;2	46.06
110	200	1079197	1 2 3 4 5	26;15;7;6;1	579846	'1 2 3 4 5'	49;32;13;12;2	46.27
120	200	993597	1 2 3 4-5	29;17;7;7;22	545324	'1 2 3 4 5'	52;35;14;13;4	45.12
130	200	901726	1 2 3 4 5	31;18;8;7;1	545324	'1 2 3 4 5'	57;35;14;18;4	39.52
140	200	836701	1 2 3 4 5	34;20;8;7;1	545324	'1 2 3 4 5'	65;35;22;14;2	34.82
150	200	790304	1 2 3 4 5	36;21;9;8;1	545324	'1 2 3 4 5'	54;35;13;21;16	31.00
160	200	735361	1 2 3 4 5	38;23;10;8;1	545324	'1 2 3 4 5'	52;35;13;18;4	25.84

[46]. As both of these methods are based on ILP, the solution is always optimal.

The overall problem could be stated as: Given a SIC with M number of dies, each die has N cores such that N_b denotes the total number of cores in die b. Each core has certain I/Os, scan chains of certain lengths and the number of test patterns to be applied. Let P_{max} denote the maximum number of pins available at the lowermost die and TSV_{max} denote the global TSV limit. Find the best possible TAM design that minimizes the OTT by:

a) Finding the 3D schedule (how dies should be tested) by optimal allocation of Test Channels (calculated using Eq. 2 and 3, for SBS) to each die such that the upper limit on P_{max} and TSV_{max} is not exceeded.

b) Finding the optimal 2D schedule (how cores within the die should be tested) such that the allocated number of channels dictated by the SIC level schedule (in part a) is not exceeded.

The optimization solution returns the TAM for the SIC which includes a 3D Schedule, 2D Schedule, and the resultant minimum possible test time (OTT). The 2D and 3D scheduling policy and the test time calculation method used in this paper is further elaborated with the help of an example in the following paragraph.

Consider the third row of Table IV which gives the optimal solution for SIC1 with 40 Pins and 200 TSVs. The optimal 3D Schedule for SBS is 1||2-3||4||5 with TAM widths of 24,14,20,16 and 2 channels, respectively, for dies 1 through 5. This implies that the 3D schedule has 2 sessions (separated by '-'); in session 1, Dies 1 and 2 will be tested in parallel using TAM widths of 24 and 14 channels, respectively, followed by session 2 in which the TAM will be reconfigured to access dies 3, 4 and 5 with 20, 16 and 2 channels respectively. The TAM width allocated to a die in a 3D schedule is further divided into sub-TAMs to form a 2D schedule. For instance, the 2D Schedules for all dies in SIC1 of the above example (row 3 of Table IV) are shown in Table V. A TAM width of 16 channels was allocated to Die4, for which the optimal 2D Schedule is '[1] || [2-3-4]' with sub-TAMs of {8,8}. This implies that the 16 channels allocated to the die are further divided into 2 sub-TAMs of 8 channels each. Sub-TAM 1 connects exclusively to

TABLE V
DIE LEVEL TAM FOR SIC 1 WITH 40 PINS AND 200 TSVS USING SBS

	Die Level Schedule	Channels	T _{die}
Die1	[5-7-10-12-16-18-24-25-26-17-29-32] [2-3-6-8-13-14-28-30] [1-4-9-11-15-17-19-20-21-22-23-31]	7,8,9	1167503
Die2	[1-4-5-8-11-15-16] [2-6-7-12-14-17-19] [3-9-10-13-18]	2,5,7	1144129
Die3	[2-3-8-10-13-14-16-17-19-20-22-23-24-27] [7-9-11-12-18-21-25-28] [1-4-5-6-15-26]	4,5,11	368546
Die4	[1] [2-3-4]	8,8	374009
Die 5	[2-3-4-5-7-9] [1-6-8-10]	1,1	332743

core 1 and sub-TAM2 connects cores 2,3 and 4 in series. The cores within a sub-TAM are tested sequentially and the test time of the sub-TAM is the sum of all core test time, i.e. $T_{sub-TAM} = \text{Sum}(T_{core})$, where T_{core} is calculated using Eq.1 for SBS. As all the sub-TAMs run tests simultaneously, the test time of the die $T_{die} = \text{Max}(T_{sub-TAM})$. Subsequently, as one or more dies may be tested simultaneously within a 3D session, $T_{session} = \text{Max}(T_{die})$; and finally, as the 3D test sessions are run sequentially, the overall test time of the SIC $OTT = \text{sum}(T_{session})$. In this way, for the given 2D schedule, the test time for Die 4 was 374009 cycles. T_{die} for the remaining dies is calculated similarly (Table V) which gives the OTT of 1541512 cycles for the given 3D test Schedule.

For simplicity, only post-bond test scenarios of soft-dies and soft-cores have been considered. Moreover, only the test time involved in the shift cycle of internal scan-test has been calculated as the rest can be ignored, being negligible. The effect of bypass flip-flops has only been accounted for SBS and ignored for UDS.

B. Results and discussion

Table IV shows the exact solutions for the OTT and the relevant schedule and channel allocation of SIC 1 using conventional and SBS based TAM when the number of pins of the bottom die is varied from 20 to 160 in steps of 10, and the global TSV limit is 200. It is evident that SBS offers significant OTT reduction; however, it may be noted that as the number of test-pins are increased, while the OTT in case of both conventional and SBS TAMs decreases (as expected), the

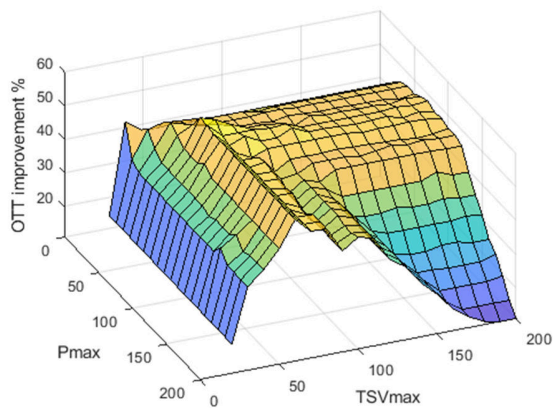


Fig. 12: % improvement in OTT of SIC 1 with varying Pins and TSV limits

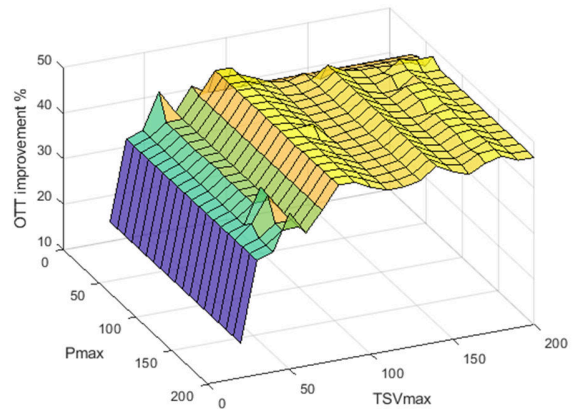


Fig. 14: % improvement in OTT of SIC 2 with varying Pins and TSV limits

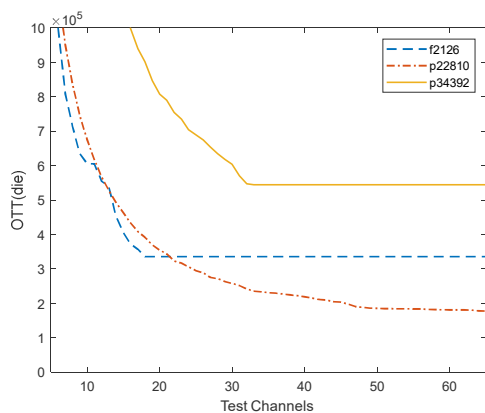


Fig. 13: Variation of the core test time with increasing number of test channels

advantage offered by SBS decreases. The effect of variation of both $P_{\max}$ and $TSV_{\max}$ on the %OTT improvement for SIC 1 is shown in Fig. 12. A maximum improvement of 53.6% could be observed when $P_{\max} = TSV_{\max} = 60$ for this particular SIC. Below this number, the advantage of using SBS decrease to 19.6% (at $P_{\max} = 20$, $TSV_{\max} = 20$). This is due to the fact that when the pin and TSV count is too low, the reference generation overheads become significant (in this case, 2 pins and 8 TSVs).

Fig. 12 also shows a decrease in the percent improvement using SBS (10.8%) as the pin and TSV limit approach 200. This could be explained using Fig. 13 in which the test times of 3 SoCs (f2126, p22810 and p34392 of the ITC'02 benchmarks) are shown against the number of channels available for testing. It can be seen that as the number of test channels is increased, the test time of the die decreases until a certain point is reached, after which there is no further decrease. In the literature, this is commonly referred to as the Pareto-optimal point, at which the T_{die} does not decrease with the increase in the number of test channels and is constrained by the length of the longest scan chain in the die cores. When using SBS, the number of test channels increase quickly with increasing pins/TSVs and reaches Pareto-optimal point much earlier. However, as pins/TSVs are increased further, the conventional TAM scheme also reaches the Pareto-optimal point, at which both schemes will have the same testing time. It may also be mentioned that

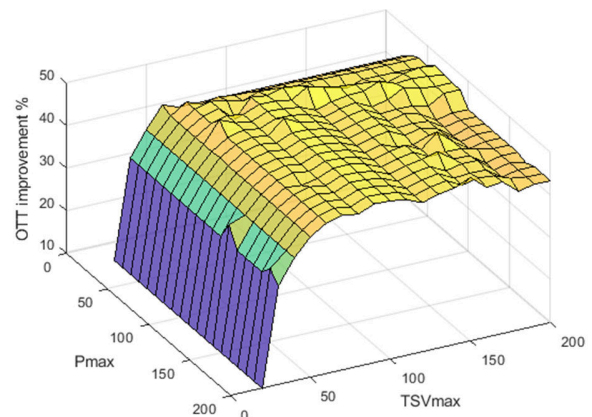


Fig. 15: % improvement in OTT of SIC 3 with varying Pins and TSV limits

at this point, the OTT of SBS may even be slightly higher due to the inclusion of die-level bypass flip-flops.

Fig. 14 and Fig. 15 show the OTT improvement using SBS for SIC 2 and 3. In both cases, a maximum improvement of around 48% percent could be observed. Unlike SIC1, both SIC 2 and 3 do not exhibit the Pareto-optimality effect at $TSV_{\max} = P_{\max} = 200$ (Pareto-optimal point does exist well beyond $TSV_{\max} = P_{\max} = 200$ but not shown for clarity). This is because SIC1 has the most complex die (p93791) placed at the bottom and benefitted directly from the increase in pin count as well as the TSV count. However, SIC 2 and 3 have the most complex die placed on top and the middle, and require a relatively large increase in TSVs to allocate more channels to reduce OTT(die). For example, to increase 1 test-channel for die 5, which is the most complex die in SIC2, at least 4 TSVs are required to be added for SBS TAM (and 8 for UDS TAM). On the contrary, if the OTT limiting complex die is the third die as in SIC3, an increase in only 2 TSVs (4 for UDS TAM) would deliver the same result. Therefore, if complex dies are higher up in the stack, a higher number of TSVs would be required to bring down the test time to the Pareto-optimal point.

The average improvement in OTT over the range of Pins and TSVs considered is 40.53% for SIC1, 42.4% for SIC3 and 43.07% for SIC2.

In order to study the offered improvement in OTT using SBS with the increasing number of dies (and hence the complexity)

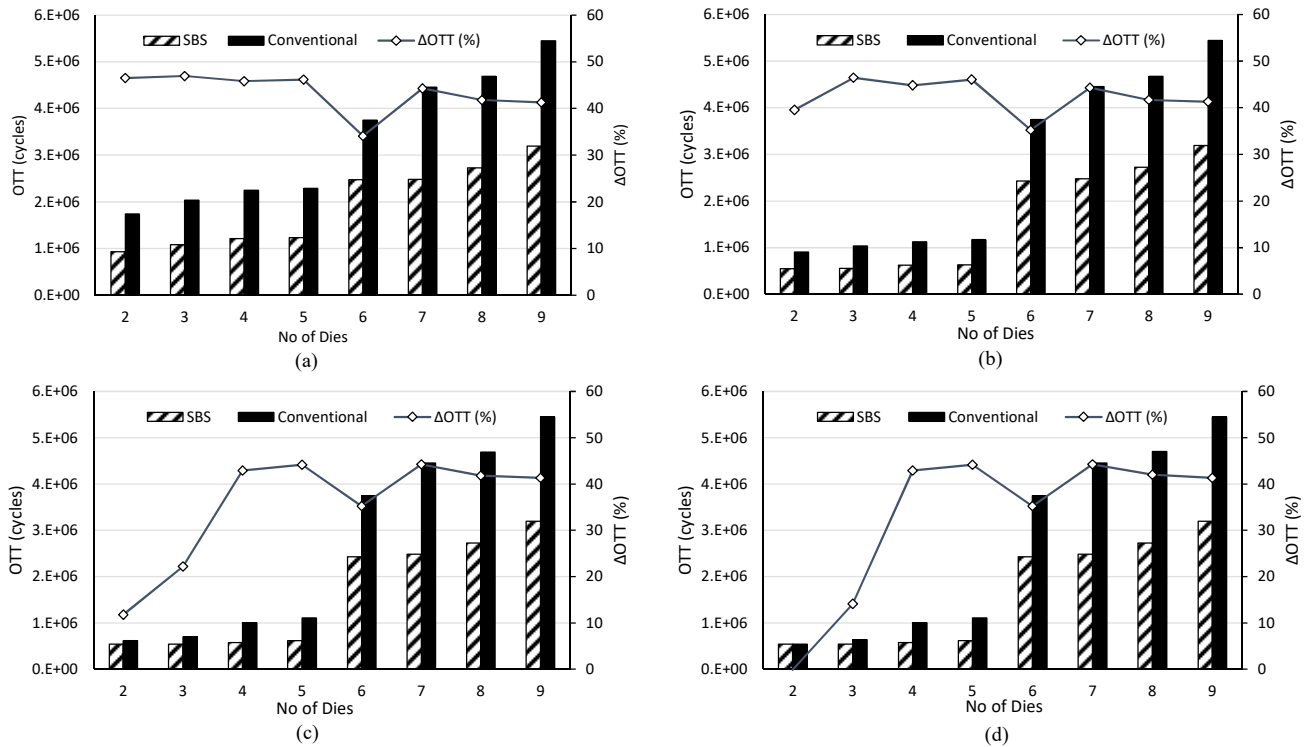


Fig. 16: Comparison of OTT and the percent OTT difference $\Delta\text{OTT}(\%)$ using Conventional and SBS based TAMs with increasing number of dies in SIC 4. Global TSV limit has been fixed to 100 and Pins equal to (a) 50 (b) 100 (c) 150 and (d) 200

of the SIC, the number of dies in SIC4 was incremented from 2 to 9 in a single die step. The global TSV limit was fixed to 100 and the percent improvement in OTT ($\Delta\text{OTT}(\%)$) when the number pins are 50, 100, 150 and 200 are shown in Fig. 16(a) through (d), respectively. It is evident that as the number of dies increase, $\Delta\text{OTT}(\%)$ also increases with the SBS approach. The relatively lesser improvement observed for dies 2 and 3 when the number of pins equals 150 in Fig. 16(c) and 200 in Fig. 16(d) is because both TAM design schemes are operating in the Pareto-optimal region. Moreover, the addition of the 6th die which is q12710 of the ITC'02 benchmark circuits, causes the relative improvement to dip down to 34% in all cases. This is due to the fact that q12710 SoC has only 13 scan-chains of lengths ranging from 413 to 1689 bits. Therefore, the test time of the SoC is now constrained by the length of the longest scan-chain of 1689 bits and remains the same as the TAM width is increased beyond 12 channels. Moreover, q12710 is placed high up in the stack and becomes the source of TSV constraint very quickly and dominates the test time for the entire stack. In all other instances, SBS offers a significant improvement of up to 46%, and hence it is clear that this scheme scales well with the increasing SIC complexity. Also, the average $\Delta\text{OTT}(\%)$ for the four cases of Fig. 16(a) through (d) are 43.37%, 42.41%, 35.45%, and 32.98% respectively, i.e. the improvement offered by SBS is more pronounced when there is a lesser number of pins, and diminished as the pins are increased. In practical scenarios, the test-channels (Pins and TSVs) are mostly very limited and that the advantage of SBS is likely to be more pronounced.

VII. CONCLUSION

A novel PTAM design method leveraging the Ternary Encoded Simultaneous Bi-direction Signaling method was proposed for test time reduction of 3D SICs. At the logic level, design considerations for the incorporation of SBS into PTAM while allowing functional mode utilization of chip terminal and co-existence with conventional uni-directional signaling based DFT resources was presented. At the circuit level, an example SBS transceiver design along with simulations was presented. At the overall test application level, experiments with 4 handcrafted 3D SICs showed a maximum improvement of 53.6% is possible. The advantage of SBS is more significant when the chip terminals are limited and scales well with SIC complexity.

REFERENCES

- [1] R. Sharma and K. Choi, "Design of 3D Integrated Circuits and Systems," in *CRC Press*, CRC Press, 2014, pp. 157–174.
- [2] G. H. Loh, Y. Xie, and B. Black, "Processor design in 3D die-stacking technologies," *IEEE Micro*, vol. 27, no. 3, pp. 31–48, 2007.
- [3] M. B. Healy *et al.*, "Design and Analysis of 3D-MAPS: A Many-Core 3D Processor with Stacked Memory," *IEEE Cust. Integr. Circuits Conf. 2010*, pp. 1–4, 2010.
- [4] C. Ababei, P. Maidee, and K. Bazargan, "Exploring Potential Benefits of 3D FPGA Integration," Springer, Berlin, Heidelberg, 2004, pp. 874–880.
- [5] U. Kang *et al.*, "8 Gb 3-D DDR3 DRAM using through-silicon-via technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 111–119, 2010.
- [6] N. A. Touba, "Survey of test vector compression techniques," *IEEE Des. Test Comput.*, vol. 23, no. 4, pp. 294–303, 2006.
- [7] J. Knechtel, O. Sinanoglu, I. (Abe) M. Elfadel, J. Lienig, and C. C.

- N. Sze, "Large-Scale 3D Chips: Challenges and Solutions for Design Automation, Testing, and Trustworthy Integration," *IPSI Trans. Syst. LSI Des. Methodol.*, vol. 10, no. 0, pp. 45–62, 2017.
- [8] H.-H. S. Lee and K. Chakrabarty, "Test Challenges for 3D Integrated Circuits," *IEEE Des. Test Comput.*, vol. 26, no. 5, pp. 26–35, Sep. 2009.
- [9] E. J. Marinissen, "Challenges and Emerging Solutions in D- and 3D-Stacked ICs," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2012, pp. 1277–1282.
- [10] S. Panth, S. K. Lim, and S. Member, "Probe-Pad Placement for Prebond Test of 3-D ICs," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 6, no. 4, pp. 637–644, 2016.
- [11] International Technology Roadmap for Semiconductors (ITRS), "ITRS 2.0 HETEROGENEOUS INTEGRATION CHAPTER: 2015," 2015.
- [12] "IEEE Standard for Test Access Port and Boundary-Scan Architecture," *IEEE Std 1149.1-2013 (Revision IEEE Std 1149.1-2001)*, pp. 1–444, 2013.
- [13] "IEEE Standard Testability Method for Embedded Core-based Integrated Circuits," *IEEE Std 1500-2005*, pp. 1–136, 2005.
- [14] E. J. Marinissen, T. McLaurin, and H. Jiao, "IEEE Std P1838: DfT Standard-under-Development," in *2016 21st IEEE European Test Symposium (ETS)*, 2016, no. 1.
- [15] M. A. Ansari, J. Jung, D. Kim, and S. Park, "Time-Multiplexed 1687-Network for Test Cost Reduction," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2017.
- [16] P. Georgiou, F. Vartziotis, X. Kavousianos, and K. Chakrabarty, "Testing 3D-SoCs Using 2-D Time-Division Multiplexing," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 37, no. 12, pp. 3177–3185, 2018.
- [17] A. Sehgal, V. Iyengar, and K. Chakrabarty, "SOC test planning using virtual test access architectures," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 12, no. 12, pp. 1263–1276, 2004.
- [18] A. Sanghani, B. Yang, K. Natarajan, and C. Liu, "Design and implementation of a time-division multiplexing scan architecture using serializer and deserializer in GPU chips," *Proc. IEEE VLSI Test Symp.*, pp. 219–224, 2011.
- [19] V. Iyengar, K. Chakrabarty, and E. J. Marinissen, "Test Wrapper and Test Access Mechanism Co-Optimization for System-on-Chip," *J. Electron. Test. Theory Appl.*, vol. 18, pp. 213–230, 2002.
- [20] Y. Huang *et al.*, "Optimal core wrapper width selection and SOC test scheduling based on 3-D bin packing algorithm," *IEEE Int. Test Conf.*, pp. 74–82, 2002.
- [21] S. K. Goel and E. J. Marinissen, "Control-aware test architecture design for modular SOC testing," *Proc. Eur. Test Work.*, vol. 2003-Janua, pp. 57–62, 2003.
- [22] E. Larsson, K. Arvidsson, H. Fujiwara, and Z. Peng, "Efficient test solutions for core-based designs," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 23, no. 5, pp. 758–775, 2004.
- [23] K. Chakrabarty, "Design of System-on-a-Chip Test Access Architecture Under Place-and-Route and Power Constraints," *Proc. IEEE/ACM Des. Autom. Conf.*, pp. 432–437, 2000.
- [24] C. Yao, K. K. Saluja, and P. Ramanathan, "Power and thermal constrained test scheduling under deep submicron technologies," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 30, no. 2, pp. 317–322, 2011.
- [25] X. Wu, Yibo Chen, K. Chakrabarty, and Yuan Xie, "Test-access mechanism optimization for core-based three-dimensional SOCs," in *2008 IEEE International Conference on Computer Design*, 2008, pp. 212–218.
- [26] X. Wu, P. Falkenstein, K. Chakrabarty, and Y. Xie, "Scan-chain design and optimization for three-dimensional integrated circuits," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 5, no. 2, pp. 1–26, 2009.
- [27] S. Deutsch, K. Chakrabarty, and E. J. Marinissen, "Robust Optimization of Test-Access Architectures under Realistic Scenarios," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 34, no. 11, pp. 1873–1884, 2015.
- [28] L. R. Dennison, W. S. Lee, and W. J. Dally, "High-Performance Bidirectional Signalling in VLSI Systems," 1992.
- [29] R. Mooney, C. Dike, and S. Borkar, "A 900 Mb/s Bidirectional Signaling Scheme," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1538–1543, 1995.
- [30] R. J. Drost and B. A. Wooley, "An 8-Gb/s/pin Simultaneously Bidirectional Transceiver in 0.35- μ m CMOS," vol. 38, no. 3, pp. 2005–2008, 2008.
- [31] H. Y. Huang and R. I. Pu, "Differential bidirectional transceiver for on-chip long wires," *Microelectronics J.*, 2011.
- [32] P. Vijaya Sankara Rao and P. Mandal, "Current-mode full-duplex (CMFD) signaling for high-speed chip-to-chip interconnect," *Microelectronics J.*, 2011.
- [33] N. Wary and P. Mandal, "Current-mode simultaneous bidirectional transceiver for on-chip global interconnects," *Proc. 6th Asia Symp. Qual. Electron. Des. ASQED 2015*, pp. 19–24, 2015.
- [34] S. Park, A. Wang, U. Ko, L.-S. Peh, and A. P. Chandrakasan, "Enabling Simultaneously Bi-Directional TSV Signaling for Energy and Area Efficient 3D-ICs," *2016 Des. Autom. Test Eur. Conf. Exhib.*, pp. 163–168, 2016.
- [35] E. J. Marinissen, S. K. Goel, and M. Lousberg, "Wrapper design for embedded core test," *Proc. Int. Test Conf. 2000 (IEEE Cat. No. 00CH37159)*, pp. 911–920, 2000.
- [36] B. Noia and K. Chakrabarty, "Pre-bond probing of through-silicon vias in 3-D stacked ICs," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 32, no. 4, pp. 547–558, 2013.
- [37] B. Noia, S. Panth, K. Chakrabarty, and S. K. Lim, "Scan test of die logic in 3-D ICs using TSV probing," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 23, no. 2, pp. 317–330, 2015.
- [38] D. L. Lewis and H. H. S. Lee, "A scan-island based design enabling pre-bond testability in die-stacked microprocessors," *Proc. - Int. Test Conf.*, pp. 1–8, 2008.
- [39] N. Wary and P. Mandal, "Current-Mode Full-Duplex Transceiver for Lossy On-Chip Global Interconnects," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2026–2037, 2017.
- [40] Y. Tomita, H. Tamura, M. Kibune, J. Ogawa, K. Gotoh, and T. Kuroda, "A 20-Gb/s simultaneous bidirectional transceiver using a resistor-transconductor hybrid in 0.11- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 627–636, 2007.
- [41] M. T. L. Aung, E. Lim, T. Yoshikawa, and T. T. H. Kim, "Design of simultaneous bi-directional transceivers utilizing capacitive coupling for 3DICs in face-to-face configuration," *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 2, no. 2, pp. 257–265, 2012.
- [42] Jae-Yoon Sim, Young-Soo Sohn, Seung-Chan Heo, Hong-June Park, and Soo-In Cho, "A 1-Gb/s bidirectional I/O buffer using the current-mode scheme," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 529–535, 1999.
- [43] G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, "Electrical modeling and characterization of through silicon via for three-dimensional ICs," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 256–262, 2010.
- [44] T. Song, C. Liu, Y. Peng, and S. K. Lim, "Full-Chip Signal Integrity Analysis and Optimization of 3-D ICs," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 5, pp. 1636–1648, 2016.
- [45] E. J. Marinissen, V. Iyengar, and K. Chakrabarty, "A set of benchmarks for modular testing of SOCs," in *IEEE International Test Conference (TC)*, 2002, pp. 519–528.
- [46] B. Noia, K. Chakrabarty, S. K. Goel, E. J. Marinissen, and J. Verbree, "Test-architecture optimization and test scheduling for TSV-based 3-D stacked ICs," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 30, no. 11, pp. 1705–1718, 2011.
- [47] P. Varma and B. Bhatia, "A structured test re-use methodology for core-based system chips," pp. 294–302, 2002.
- [48] E. G. Coffman, Jr., M. R. Garey, D. S. Johnson, and R. E. Tarjan, "Performance Bounds for Level-Oriented Two-Dimensional Packing Algorithms," *SIAM J. Comput.*, vol. 9, no. 4, pp. 808–826, Nov. 1980.



DSPACE

<https://dspace.org/>

Test time reduction of 3D stacked ICs using ternary coded simultaneous bi-directional signaling in parallel test ports

Soomro, Iftikhar A.; Samie, Mohammad; Jennions, Ian K.

2020-03-03

IEEE

<https://doi.org/10.1109/TCAD.2020.2977604>

Soomro IA, Samie M, Jennions IK. (2020) Test time reduction of 3D stacked ICs using ternary coded simultaneous bi-directional signaling in parallel test ports. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 39, Issue 12, December 2020, pp. 5225-5237