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Procedia CIRP 59 (2017) 280 – 285

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The 5th International Conference on Through-life Engineering Services (TESConf 2016)

A brief overview of SiC MOSFET failure modes and design reliability

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Abstract

This paper briefly introduces various aspects which should be considered when implementing Silicon Carbide (SiC) based metal-oxide-semiconductor-field-effect-transistors (MOSFETs) into a design. There is an increasing trend regarding the use of these devices in various applications due to their improved performance over conventional Silicon (Si) based devices. The failure modes of SiC MOSFETs are discussed, as well as the indicators which signal device degradation and failure. The impact of packing design on reliability and performance is also discussed along with a number of application related concepts which bring to light some of the issues regarding the use of SiC MOSFETs as a relatively young technology.

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Peer-review under responsibility of the scientific committee of the The 5th International Conference on Through-life Engineering Services (TESConf 2016)

Keywords: SiC, MOSFET, Overview, Reliability, Failure, Application

1. Introduction

Cost, efficiency, power density, complexity, and reliability; these are some of the major factors that must be taken into account throughout the design and development of any power electronics system. The consideration of these factors enables an engineer to develop the most suitable product to meet a specific requirement without over-engineering the solution.

The commercial availability of Wide Band Gap (WBG) semiconductor devices has begun to allow design engineers a few more freedoms during the design stages of a product due to their ability to operate at higher temperatures, voltages, and frequencies compared to their Silicon based counterparts. Silicon Carbide (SiC) is one such type of WBG material, along with Gallium Nitride (GaN) and others which are not covered in this review.

Silicon Carbide based devices have been available to design engineers since the release of the first commercially produced SiC Schottky Barrier Diodes (SBD) in 2001. 5th generation SiC SBDs are available at present, alongside MOSFETs, JFETs, and Hybrid SiC-IGBT modules. The rapid growth of SiC-based devices can be attributed to the performance increases that have been repeatedly demonstrated in the various literature, with more applications being found that can benefit from the use of SiC in various parts of their design.

In general, the characteristics of SiC devices which make them most appealing compared to more conventional Silicon (Si) based devices, is the ability to operate at higher temperatures, increased blocking voltages, lower static losses and improved dynamic performance. In Fig. 1 a comparison is given between a Si-IGBT and SiC MOSFET of similar rating, illustrating the reduction in overall losses for switched type application.

A number of manufacturers have released SiC-based devices which allow for greater flexibility during the design stages of new power electronics products. The long-term goal of the power electronics industry is to embed power electronics into various applications which can benefit from their use by way of increased efficiency, reduced overall volume, and improved performance.

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doi:10.1016/j.procir.2016.09.025

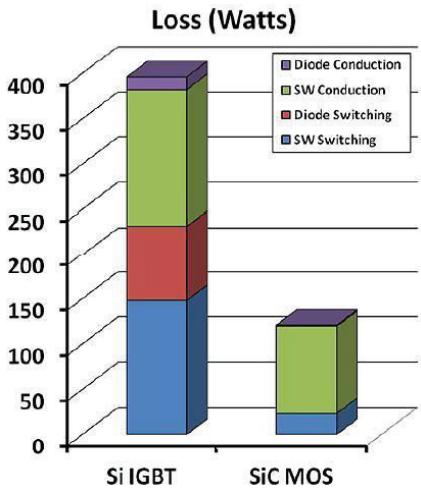


Fig. 2. Loss comparison between Si and SiC devices of similar ratings [9].

Since the design of SiC on a device level is typically a trade-off between static and dynamic behavior performance, we can expect an increased variety of available products in the coming years to suit a variety of markets and applications.

2. Failure Symptoms of SiC MOSFETs

2.1. Gate threshold voltage degradation

The reliability of SiC MOSFET gate oxides has been a frequent topic of discussion in papers over the last two decades. This is mainly due to the smaller thickness of the gate oxide layer and the relatively higher electric field applied, compared to Si MOSFETs. In the case of SiC MOSFETs, a high electric field is typically taken as the maximum recommended gate voltages of -20V for the OFF state and +20V for the ON state. When either of these voltages is applied for long periods, it has been shown in the literature that the threshold voltage increases with time. This effect has been reduced in 2nd Generation SiC MOSFETs but a change of approximately 0.25V can be expected.

At present, the recommended gate voltages for SiC MOSFETs are typically -5V and +20V. This may cause some alarm for design engineers regarding the statement above but it has been shown in the literature that while the threshold voltage will change after applying a high gate voltage for a prolonged period, the change is reversed when an opposite gate voltage is applied.

In essence, this means that for switched applications where the gate voltage will regularly alternate between ON and OFF values, any small change in the threshold voltage will be of little consequence. However, applications which will see operation for prolonged periods in the ON or OFF state must be carefully considered to determine if the change in threshold voltage will have an impact on the operation of the design. A typical example of this would be the use of MOSFETs as DC circuit breakers, as demonstrated in [1], where the reaction

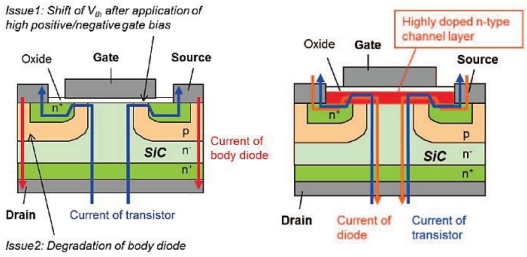


Fig. 1 (Left) DMOSFET Structure. (Right) DioMOSFET structure proposed [2].

time of the system is critical in order to protect other systems in the case of a fault.

Steps are being taken by semiconductor manufacturers to optimise the production processes of gate oxide and reduce the number of impurities in a given area. It has been shown in [2] that the introduction of a highly doped n-type channel layer to the MOSFET structure is able to minimize the change in threshold voltage when the device is stressed. This proposed DioMOSFET structure is shown on the right in Fig. 2.

Also, it has been shown in [3] that current gate oxide technology can achieve long-term reliability at high-temperature operation if the stress on the gate oxide is maintained to within tolerable levels. This translates to careful design of the gate drive voltages for a given system.

So while it can be said that the gate oxide technology is in need of optimisation, it is not inherently unreliable provided that certain aspects are taken into account when implementing SiC MOSFETs.

2.2. Body diode degradation

Consider the MOSFET structure shown in Fig. 2 (Left). A PN-junction can be seen, which makes up the essential requirements for an anti-parallel diode, referred to as the body diode, which is common to the majority of MOSFET designs available today and is typically used as a path for flyback energy in switched circuits.

It has been shown in [2,4,5] that the body diode degrades under continuous forward current, resulting in higher forward voltages and ultimately higher power dissipation during conduction at a given current.

The typical response to this problem has been the addition of a SiC Schottky Barrier Diode (SBD) which has a lower forward voltage and faster recovery time. The addition of an SBD provides an alternative path for any flyback currents, thus slowing the degradation of the body diode. The SBD comes with a cost, namely in the form of additional SiC substrate, which increases the overall production cost of the SiC MOSFET.

In [2] it was shown that the addition of an n-type channel layer could improve the reliability of a SiC MOSFET with regard to the change in the gate threshold voltage. It was also shown that the addition of this layer provides an alternate current path for reverse currents, thus preventing degradation

of the body diode. This can be seen in Fig.2 (Right). Testing of the proposed design showed very little change in the diode conduction performance, thus increasing the inherent reliability of the design.

The additional cost of the proposed design is lower than that of the additional SBD approach since the n-type channel layer forms part of the design of the MOSFET and does not require additional SiC substrate.

From an application perspective, the choice of the SiC MOSFET for a given design will need careful consideration as to the how often the MOSFET will experience reverse conduction conditions and whether or not a fully rated diode structure is needed.

2.3. Increased Gate leakage current – A sign of device failure

Consider that a number of Switch Mode Power Supply (SMPS) designs require that the switching device is cable of handling pulse currents which could be greater than 4x the nominal rating of the device. In other cases , a switching device would be expected to cope with short-circuit currents of more than 10x the rated current for a brief period, especially if the application formed part of a protection system such as a DC circuit breaker.

Similarly, SiC MOSFETs are expected to survive under these types of switching conditions, and so the stresses that are placed on the device must be considered. Examine Fig. 3, which shows the voltage and current waveforms of a 1200V 150A SiC MOSFET under pulse test conditions as given in [6], it can be seen that the device experiences peak currents of 600A or 4x the nominal rating of the device. The inset graph shows the power dissipated in the device during each switching event, which reaches a peak of 90kW. This causes a rapid temperature rise inside the device. This effect is greater under short circuit conditions, where very high currents are likely to flow.

In [6] it was shown that during a short circuit event the entire DC bus voltage is seen across the device. This causes an electric field to be applied which, at sufficiently high levels, is able to cause a reach-through effect. This causes high leakage currents to flow from the gate to the source. This effect depends on the thickness of the gate oxide layer and the strength of the applied electric field, so the results will vary depending on application and MOSFET design. It must be noted that the gate oxide layer thickness of SiC MOSFETs is lower than that of Si MOSFETs, and so are particularly susceptible to this effect.

The temperature rise experienced by the device, as a result of the short circuit event, causes additional leakage currents to flow. The result of the event is degradation of the gate oxide since the leakage current is forced to flow through this layer between the Gate and Source of the device.

Each repeated high current event causes further degradation of the gate oxide layer, increased leakage currents, and eventually a total failure of the gate will occur. It then follows that switching frequency is an important factor in pulsed current designs since a higher operating frequency would mean a greater number of pulsed current events and so will result in faster degradation.

It thus becomes necessary to either factor this failure mode into the design of the system or to integrate a Gate current measurement system which is then able to determine the health of the device by monitoring the level of leakage current during each switching event.

2.4. Avalanche events

An avalanche event is likely to occur in designs which involve switching current through an inductive circuit element, such as the one shown in Fig. 4. It is the result of the energy stored in the inductive load which, when released, generates a voltage spike greater than the breakdown voltage of the switching device.

Typical inductive switching designs such as flyback converters are designed such that the voltage rating of the device exceeds that of the expected voltage spike since the stored energy is transferred to the load. It is not uncommon though for devices to be subjected to unexpected voltage spikes due to stray inductances in current paths and other similar elements. In other cases, such as regenerative braking, an avalanche condition is expected and factored into the design.

The nature of an avalanche event is such that the voltage spike exceeds the breakdown voltage of the device, which then allows current to flow through the MOSFET, dissipating power and creating a sudden rise of the internal temperature.

Most importantly, the current that flows through the device during such an event causes degradation to the layers of

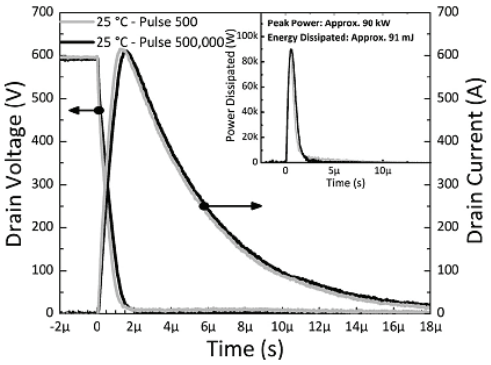


Fig. 3. Pulse test waveforms. (Inset) Power dissipated during pulse.[5]

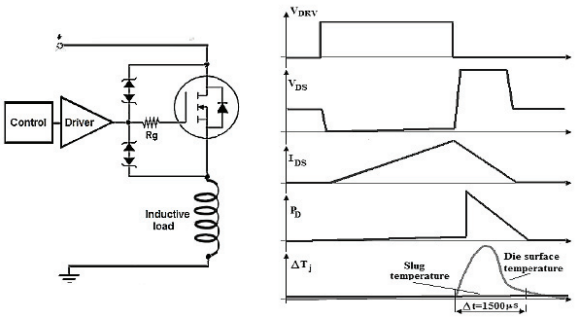


Fig. 4. Inductive switching test circuit and illustrative waveforms [7]

material in the current path. This degradation has the measurable effect of increasing the Rds(on) value of the device. Further degradation occurs during each successive avalanche event and so the Rds(on) will increase as well.

The implication of this is that the power dissipated by the device during the ON state will increase and will thus require additional cooling in order to maintain a safe operating temperature. This increase in power dissipation can and should be included at the design stage of a system by means of extra cooling to account for the increase over time.

It has been shown in [7] how avalanche events affect a SiC MOSFET as well as how the degradation can be modelled and predicted over the life of a design. While avalanche events are not unique to SiC-based designs, they still play an important role in determining the reliability of design especially considering the prevalence of power electronics in the world today.

3. Packaging reliability

One of the aspects of power semiconductors that must be considered is the packaging of the devices.

In order to make the most out of Wide Band Gap materials in application, the packaging of the devices needs to be reconsidered. The conventional structure of existing Si and SiC power modules means that the current paths are formed by means of Aluminium (Al) bonding wires which connect the terminals of the package to the semiconductor die. This die is soldered to a direct copper bonding substrate (DCB) which in turn electrically isolates the die from the base of the package while still providing sufficient thermal transfer of heat. All of the components are then encapsulated with Silicone gel in order to provide protection against environmental effects, such as humidity and dirt.

In [8] it was demonstrated that the overall packaging methodology of semiconductor power modules could be improved in order to achieve higher performance from the devices while also reducing the overall size of the packaging. This is a crucial point since it implies that the power density of a design can be increased.

The number of Al bonding wires used inside a power module increases with the number of dies that is interconnected. As the current carrying requirement of the module increases, more bonding wires need to be connected in parallel and more area has to be provided on each die for the physical connections.

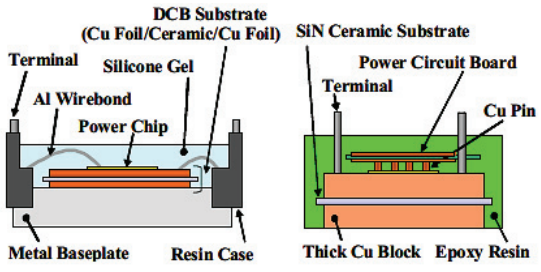


Fig. 5. (Left) Typical and (Right) proposed power module structures [8]

The new packaging method suggested in [8] introduces the concept of using a power PCB (Printed Circuit Board) to provide the interconnections between each die and the terminals of the package. The connections are made by means of Cu (Copper) pins and tracks. This concept allows for shorter current paths and since Cu has a higher conductivity compared to Al, the ohmic and inductive losses are reduced. A comparison between a conventional power module design and the proposed design can be seen in Fig. 5.

This translates into a smaller volume required for a given number of interconnections, which reduces the overall size requirement of the package without compromising the performance of the semiconductor.

Epoxy resin was proposed as the encapsulation material due to its stability at high temperature as well as its mechanical stability in the hardened state. This reduces the mechanical stresses experienced by the module as a result of temperature changes and vibration, thereby increasing long term reliability.

It was shown how the overall thermal resistance of a power module can be reduced by making use of new materials and methods. This allows the package to operate at higher temperatures than would have been previously possible, which improves reliability and enables new applications.

It was also shown in the literature that the switching losses of a device could be reduced by the modifications to the packaging method. These reductions are believed to be the result of the shorter current paths, which exhibit lower parasitic inductances due to their laminated structure.

Together, all of these proposed changes result in making better use of the characteristics of SiC devices and the improved performance of power modules in general.

4. Design reliability, protection schemes and health monitoring

4.1. Electromagnetic Compatibility (EMC)

One of the greatest benefits of using SiC MOSFETs is their low switching energy. This allows the use of higher switching frequencies in application to reduce the size of passive components required for filtering.

Part of the requirements for the reduction of switching losses is the use of high-speed gate drive circuitry. This is needed to charge the gate capacitance of the MOSFETs in the shortest possible time and thus reduce the energy dissipated during each switching action.

The result of the high-speed switching is an increased Electromagnetic Interference (EMI) signature due to the high rate of change (di/dt) values present when charging and discharging the gate capacitance of the MOSFETs, as well as the high-speed switching of the load current. The magnitude of EMI increases with the amount current being switched and with the speed at which the switching occurs.

An increased EMI signature can lead to noise, instability and unexpected behavior of the control circuitry used in the system, so it is vital that adequate protection is put in place

during the design stage to prevent any interference from having a detrimental effect.

4.2. Ringing / Overshoot

The effect known as ringing is essentially an overshoot of the voltage across a switching device. It is caused by the high speed switching transient of a device which provides excess energy to the parasitic inductance and capacitance present in the circuit. This creates a resonant interaction which generates a high voltage oscillation that can easily exceed the voltage rating of the device, causing damage and possible failure. Refer to Section D. Avalanche Events for further detail on this particular failure mechanism.

The primary sources of the excess energy are high di/dt and dv/dt values which are present when a device switches. These values can be reduced by slowing the rate of switching which then provides less energy to the parasitic elements.

It must be noted that the act of slowing the switching speed of a device will increase the switching power losses.

Alternatively, ringing can also be minimized by reducing the parasitic elements present. Circuit layout tends to be the primary cause of parasitic elements, so care needs to be taken during the design stage in order to minimize their effect.

This can be achieved through a variety of methods, such as reducing the current path length which reduces the stray inductance of the path or selecting a switching device which has the lowest possible output capacitance.

A further solution is the addition of snubber circuitry which is used to provide a dissipation path for the excess energy. The energy is dissipated in the form of heat and is thus wasted. Applications which have a focus on efficiency would typically avoid the use of snubbers wherever possible.

The presence of ringing will increase the EMI signature of a design and can lead to instability of the control system.

4.3. Short circuit detection and protection

In many switched applications, it is likely that the switching device will encounter a short-circuit event. This can be caused in a number of ways such as cross-talk between devices in a phase leg configuration, a short-circuit at the output or noise in the control circuitry.

Regardless of the cause, an uncontrolled short-circuit event can cause serious damage to a system as well as to sensitive loads. Thus it becomes necessary to protect the system against such events.

SiC MOSFETs are especially susceptible to damage as a result of short-circuiting events due to their fast switching speeds and very low on-state resistance. It has been shown in the literature that the current passing through a SiC MOSFET can exceed 10x the nominal rating with 10-20µs after turn-on, which implies that the time needed to detect and react to short-circuit events is very small.

The methods of detecting such events for slower devices are well documented and similar methods can be applied to SiC MOSFETs with little alteration.

The primary method of detecting short-circuits is the measurement of VDS (SAT) which is the voltage across the Drain and Source of the MOSFET after it has reached the on-state. This voltage follows Ohm's law, meaning that it is directly related to the on-state resistance of the device and the current flowing through it. If it is assumed that the on-state resistance of the device is constant, then the current through the device can be estimated.

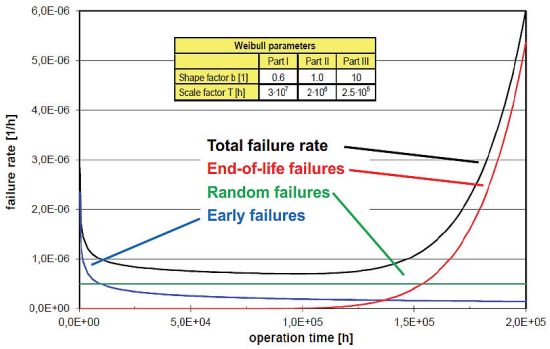


Fig. 6. Failure rate of power devices during operational lifetime [11].

A typical detection circuit will compare the VDS (SAT) with a preset value; if this value is exceeded then gate drive circuitry will be inhibited or changed to the off-state.

In order for a similar method to be used with SiC MOSFETs, the detection and reaction time must be as fast as possible. In the literature, it has been shown that a response time of 2-5µs is sufficient to protect the device.

A number of manufacturers now offer gate driver solutions for SiC MOSFETs which allow for high-speed switching as well as short-circuit protection.

4.4. Burn-in testing

Consider Fig. 6 and note, in particular, the early failures. These are typically due to defects in the system as a result of some inconsistency during the manufacturing process. This can relate directly to the power devices themselves as well as the system in which they are used.

A high early failure rate can result in extra time and cost being added to a project in order to repair/replace systems which have failed.

It is possible to reduce the early failure rate of a given design by incorporating a burn-in test as a part of the manufacturing and testing process. The purpose of a burn-in test is to subject a system to the stresses that it would be expected to handle under normal operation conditions.

By monitoring critical parameters during the stress test it is possible to determine any variance/change. This variance is then compared to a specific acceptance window and if the variance exceeds the acceptance window, then a decision can be made regarding the usage of that particular system in an application. A rigorous stress test can also alert the design engineer of any issues or faults inherent to a specific design before mass production is reached.

While it is expected that more modern devices and designs will be more reliable than in the past, it is prudent to have a pro-active method of preventing failures in the field.

4.5. System level monitoring

Consider again Fig. 6 and note the non-zero value of the total failure rate as well as the rapid rise in end-of-life failure rate after 125 000 hours of operation.

It can be seen that no single system has a zero chance of failure and depending on how critical the application is it would be useful to know the current health of the system as well as to estimate its remaining useful life.

This estimation can be made using prediction of failure methods which use system data to determine any degradation or variance in critical parameters such as; gate drive voltage, gate threshold voltage, gate leakage current, VDS, VF(diode) , efficiency, temperatures and device current.

It is not always cost effective to monitoring every available parameter of a system. Depending on the most likely cause of failure for a given design as well as the key performance characteristics, a few specific parameters can be chosen for monitoring and measurement.

5. Summary

The purpose of this paper was to introduce the reader to some of the aspects and issues concerning the use of SiC MOSFET devices in application. Failure modes and symptoms were discussed, to illustrate how the degradation of the devices can be measured and estimated. Some packaging reliability aspects were briefly covered and it was seen that there are gains to be had by adopting packaging which is capable of high-temperature operation. Some design reliability concepts were discussed in order to illustrate how device failures can be reduced in the field by taking into account the required operation characteristics during the design stage. Further reductions can be had by incorporating stress tests during the production phase of a design. Additionally, using the failure symptoms discussed initially, the health of a system can be estimated by monitoring key parameters and incorporating prognostic algorithms.

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2017-03-02
Elsevier
http://dx.doi.org/10.1016/j.procir.2016.09.025
Nel BJ, Perinpanayagam S, A Brief Overview of SiC MOSFET Failure Modes and Design Reliability, Procedia CIRP, Volume 29, 2017, Pages 280 - 285.

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